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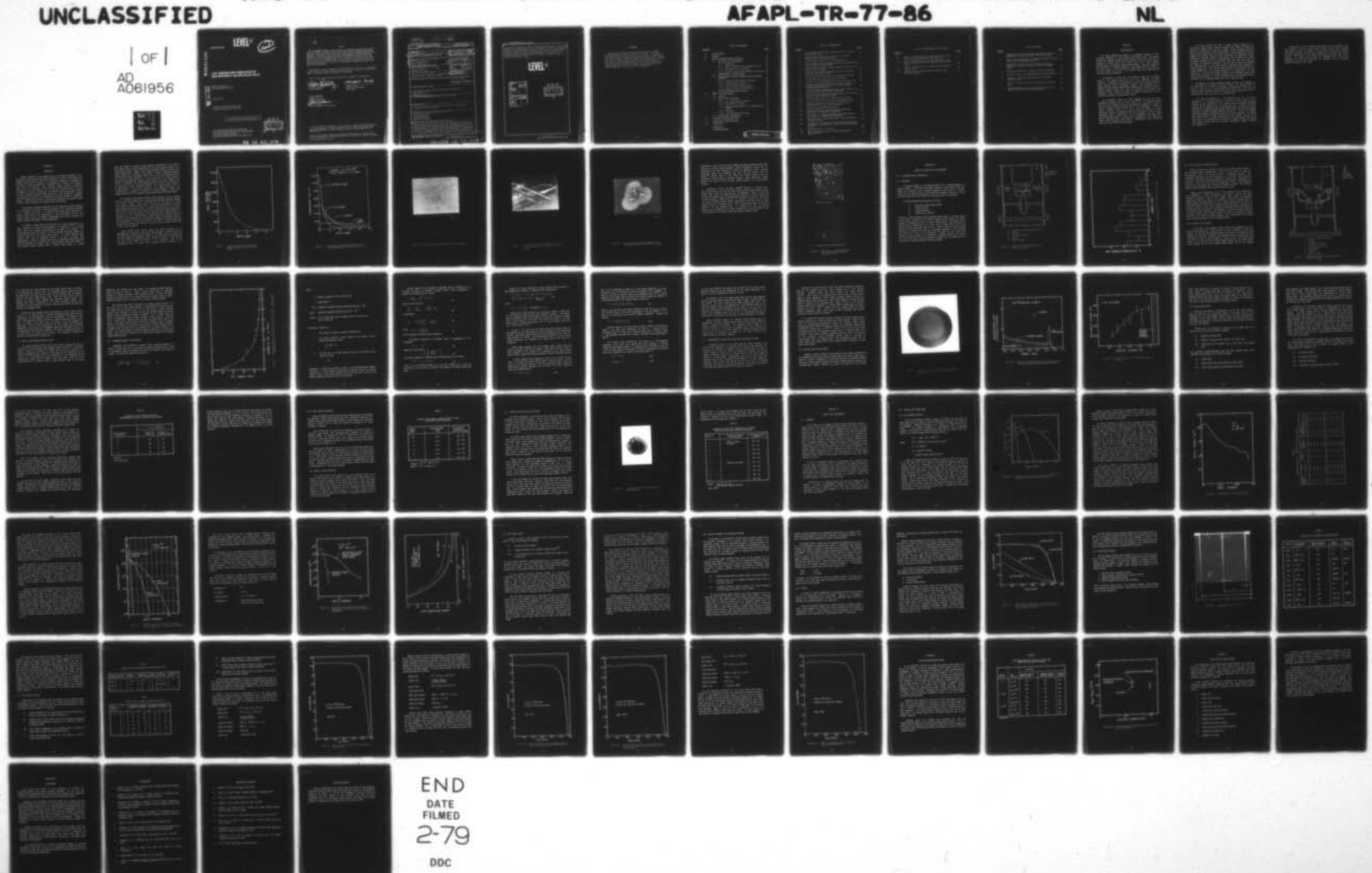

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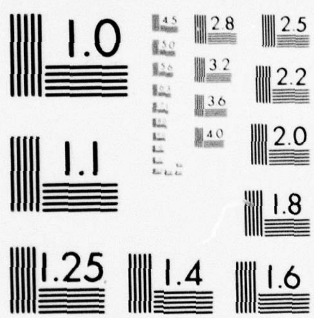
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LEVEL II

AFAPL-TR-77-86

LOW TEMPERATURE FABRICATION OF HIGH EFFICIENCY SILICON SOLAR CELLS

SPIRE CORPORATION
BEDFORD, MASSACHUSETTS

AUGUST 1978

TECHNICAL REPORT AFAPL-TR-77-86
Final Report February 1975 – June 1978

Approved for public release; distribution unlimited.

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W. Patrick Rahilly
Project Engineer

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Technical Area Manager
Solar Power

FOR THE COMMANDER

James D. Reams
Chief, Aerospace Power Division

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This report describes the results of a program to develop ion implantation/pulsed energy processing for spacecraft solar cell applications. The approach involves employing pulsed electron beam technology to achieve processing parameters not previously possible by conventional furnace heat treatments. Optimization of the ion implanted solar cell structure was undertaken but not completed. Cells with efficiencies to 13.7% AMO were achieved

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using furnace annealing and to 12.9% AMO using pulsed electron beam annealing. Prospects for future development to higher efficiencies and for totally automated production are excellent. Experimental evidence suggests that the ion implanted, pulsed electron beam annealed solar cell may have better inherent tolerance to electron irradiation than similar diffused or furnace annealed implanted junction cells.

LEVEL II

FOREWORD

This Final Technical Report was prepared by SPIRE Corporation under Contract F33615-75-C-2006. The effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio under Project 3145, Task 314519 and Work Unit 31451951 with Dr. W. Patrick Rahilly/POE-2 as Project Engineer. The program was initiated with FY75 Air Force Aero Propulsion Laboratory Director's Funds. Alan Kirkpatrick of SPIRE Corporation was Principal Investigator.

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SECTION I

INTRODUCTION

This report describes the results of a development program for "Low Temperature Fabrication of High Efficiency Silicon Solar Cells". The program involved was conducted primarily between February 1975 and June 1977 but was continued at minimal effort level through June 1978 to allow adequate characterization of substantial developmental successes. This study represented the initial work on a radical approach to cell processing which is expected to have major impact on the cost of space qualified solar cells through improved yield and conversion efficiencies.

The approach to silicon solar cell fabrication which was the primary subject of this program involves the use of ion implantation for dopant introduction in conjunction with applications of directed energy pulsed heating to replace standard elevated temperature processes. The combination of ion implantation with submicrosecond localized pulsed energy techniques provides a powerful capability around which solar cell fabrication can be based. This technology is now becoming the subject of intensive developmental work for applications throughout the semiconductor industry.

Ion implantation itself has been employed for solar cell source developmental purposes since the early 1960's [1,2,3]. Ion implanted junction solar cells have exhibited performance characteristics comparable to those of similarly structured diffused junction cells. If ion implantation is treated as simply a substitute process to be used in place of diffusion for dopant introduction purposes, ion implanted cells can be expected to have the same performance limits as diffused cells. But ion implantation does offer several distinct advantages relative to diffusion and, if implantation is fully exploited by basing a total fabrication scheme around it, possibilities do exist for achieving nearly ideal cell structures and performance.

It has been primarily the need to anneal radiation damage to the semiconductor crystal lattice caused by implanted ions which has limited the potential of implantation for solar cell purposes. Standard annealing procedures involve furnace operations at temperatures similar to those employed for junction diffusions and annealed layers are often characterized by appreciable residual imperfection. The basic objective of this program was to develop a new method of damage annealing for the ion implanted solar cell which could avoid the deficiencies of conventional techniques. This new method involves the implanted layer being subjected to a very brief transient temperature spike produced by a directed energy pulse. The surface heating transient can be generated by use of a high intensity burst of low energy electrons or by a pulsed laser. The main requirement is that the pulsed energy be absorbed in the localized vicinity of the surface being processed in a period sufficiently short that appreciable thermal conduction from the deposition region cannot occur during the pulse.

Development of the pulse annealing technique has been very successful. It has been found to be possible to produce annealed ion implanted solar cell junctions which are free of polycrystallites and dislocations. Even the best furnace annealed implanted junction layers always exhibit appreciable densities of dislocations and usually some presence of polycrystallites.

The plan for optimization of the implanted solar cell has involved development of a complete process in which the cell base region is never subjected to high temperatures. It is believed that all elevated temperature processes can be replaced by use of pulsed energy steps. In addition to use for annealing of ion implanted layers, pulsed electron beams have under this program been used to replace sintering operations for contacts. A basis for simplified automated production of spacecraft solar cells has been established. The program also included efforts to begin optimization of the complete structure of the silicon solar cell. Consideration has been given to junction profiles, back surface layer doping, contact design and materials, antireflective coatings, texturized front surfaces, etc.

Development of the ion implanted cell structure is not yet complete. Best cells fabricated under this program were relatively simple without complete optimization of structure or process. But these cells with efficiencies exceeding 13% AMO demonstrate that very high performance ion implanted cells will be achieved. This program has provided the groundwork upon which future development of very high performance ion implanted cells and automated production processing will be based.

SECTION II

APPROACH

Specific objectives of this program were (i) to develop technology for low temperature pulsed electron beam process fabrication of N^+/PP^+ high efficiency ion implanted silicon solar cells and (ii) to demonstrate feasibility of employing this technology for high rate production of spacecraft cells. Methods were developed which allow cell fabrication under conditions whereby maximum temperature experienced by the base region of the cell could be arbitrarily limited. This was accomplished by using ion implantation in combination with pulsed energy methods to replace necessary operations usually performed at high temperature. Emphasis of the program was upon the ion implantation and pulsed annealing of implantation damage. Consideration was given to identifying requirements and processes which will lead to high performance ion implanted solar cell structures.

Pulsed energy processing, particularly for ion implantation damage annealing, is a key element in achieving an effective approach to low temperature processing of high efficiency solar cells. It is apparent that pulsed energy annealing is to become widely used for ion implantation of many semiconductor devices. This program involved much of the original developmental work on what is expected will become important technology for general applications.

To perform a pulsed energy step which does not elevate temperature of the entire structure of the device being processed, it is necessary to use an energy source which can be absorbed preferentially in the region to be processed. The pulse duration must be short relative to the time required for thermal energy to be conducted away from the volume being treated. The locally absorbed, short duration pulse must be sufficiently intense to be able to produce high temperatures. A number of energy sources can be considered including lasers, high intensity flashlamps and electron beams. Pulsed electron beams were utilized in this program because facilities able to process 2-inch wafers in a single

pulse were available and because energy deposition characteristics of the electron beam depend upon the electron parameters not upon the crystalline condition of the material being treated. Figure 1 shows energy deposition profile in silicon of the pulsed electron beam employed in this program. Figure 2 illustrates calculated resulting surface region temperature profiles at the end of the 100 nanosecond pulse and at several instants thereafter. It can be seen that the silicon surface is subjected to extremely high temperature which relaxes with a time constant of the order of a microsecond. At depths appreciably below the surface the material does not experience any major temperature elevation. The condition shown in Figure 2 is representative of good pulsed annealing of ion implantation damage. The implanted layer is subjected to instantaneous melting resulting in liquid phase epitaxial regrowth from the undamaged silicon crystal below the implanted region.

The conditions which produce effective pulsed annealing of an ion implanted layer are not widely separated from conditions which can cause permanent damage to the silicon. Figure 3 shows a microscopic view of the surface of a silicon wafer exposed to excessive pulse fluence. In this case microcracking of the wafer along crystal planes has taken place. The pulsed beam must also be kept uniform. Figure 4 shows an example of localized surface mechanical damage produced by a "hot spot" in a beam and Figure 5 shows localized surface melting caused by a filamentary arc in an electron pulse. Electron beams were developed under the program to allow processing over 2-inch diameter regions with sufficient uniformity and reproducibility to avoid such problems. The ability to produce large area uniform beams represents the advantage of electron beams over lasers which might be used for similar purposes.

High intensity pulsed electron beams can contain quantities of ions originating from components of the electron beam generator. If present, these ions can impact upon, and penetrate the surface of, the wafer being processed and can cause cell performance degradation effects. During the program it was found that cell open circuit voltage is sensitive to ion contaminants. Much of the developmental work on electron beam conditions involved reduction of ion

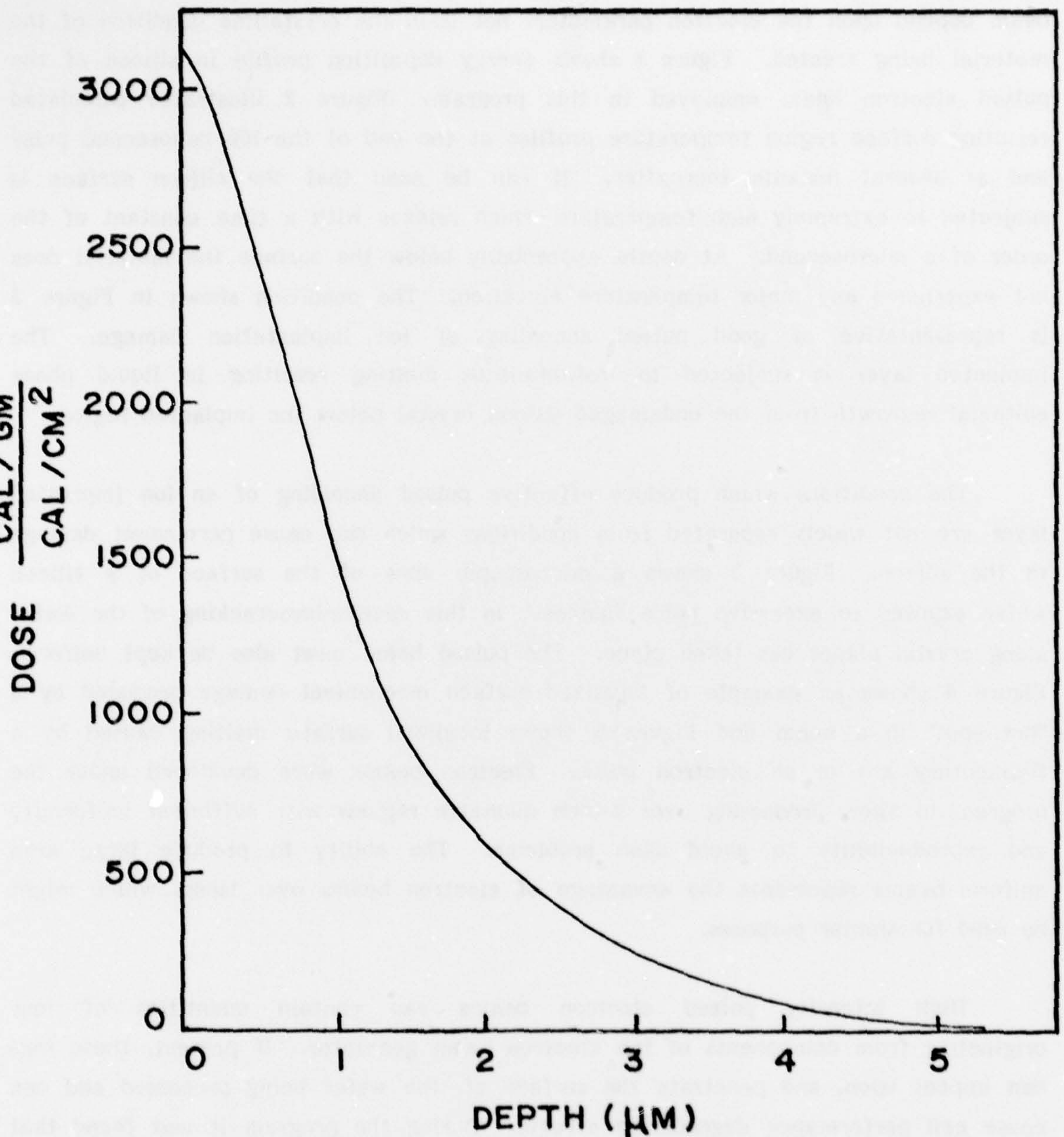

Figure 1. Energy Deposition Versus Depth Profile in Silicon for Electron Beam

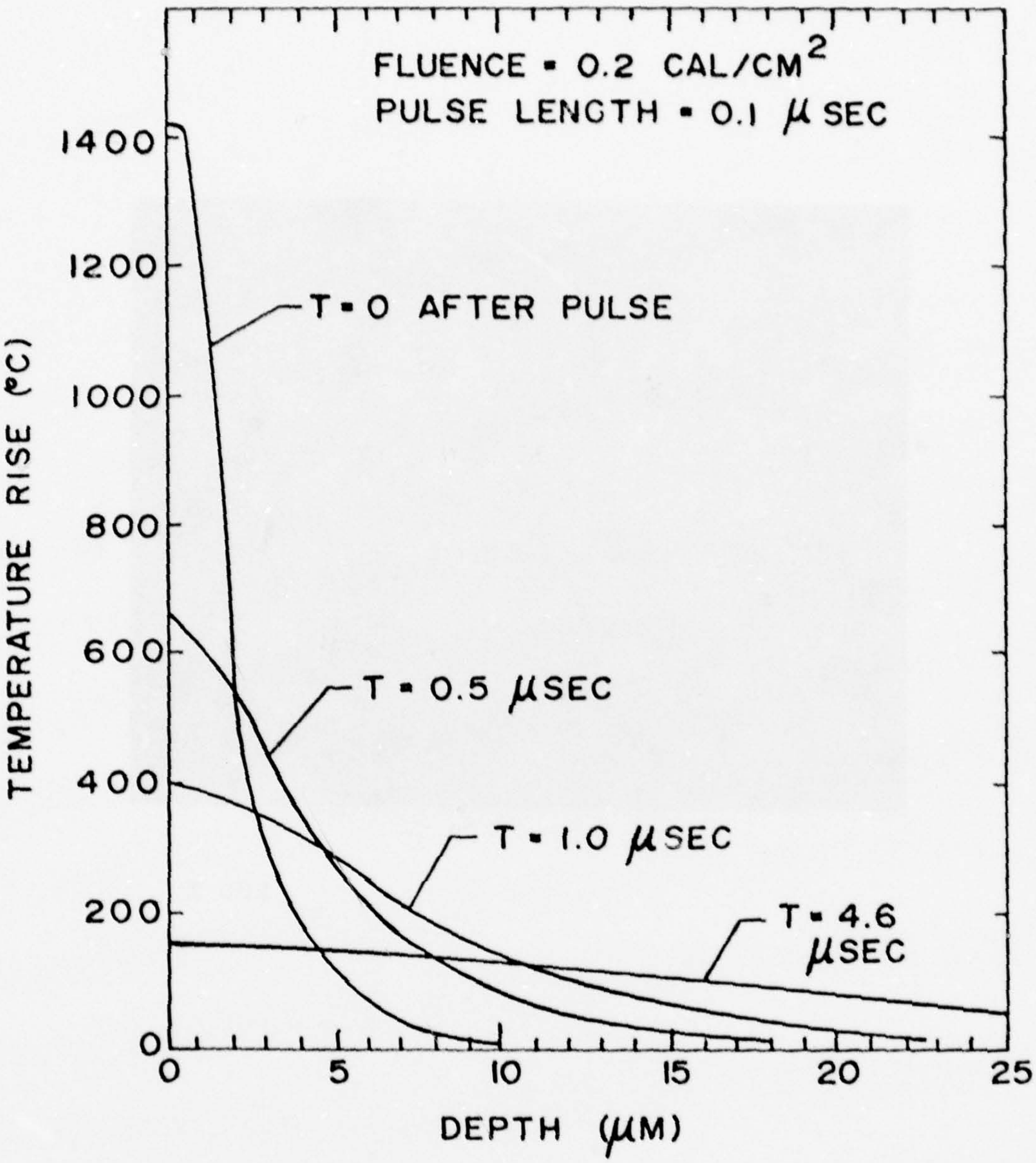

Figure 2. Instantaneous Temperature Profiles in Silicon Produced by Electron Beam Pulse

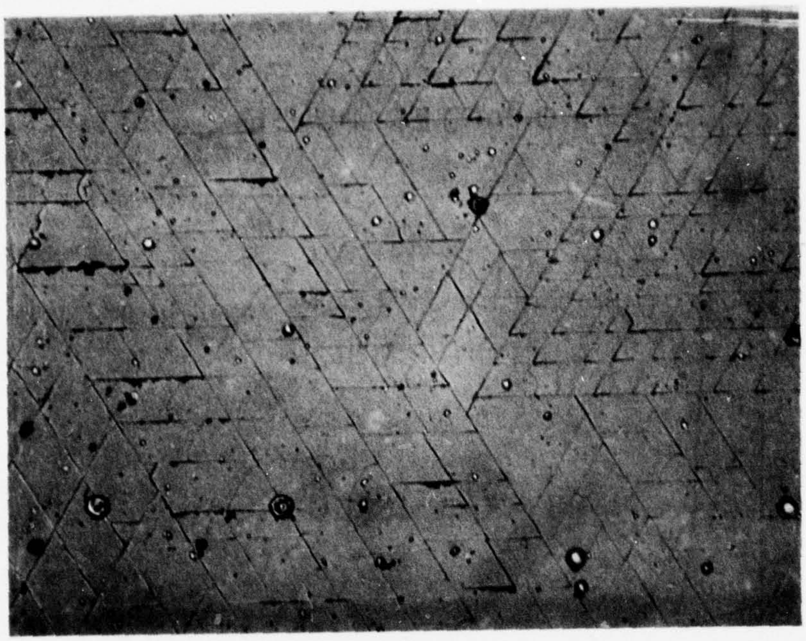

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Figure 3. Microfracture Pattern on Silicon Surface

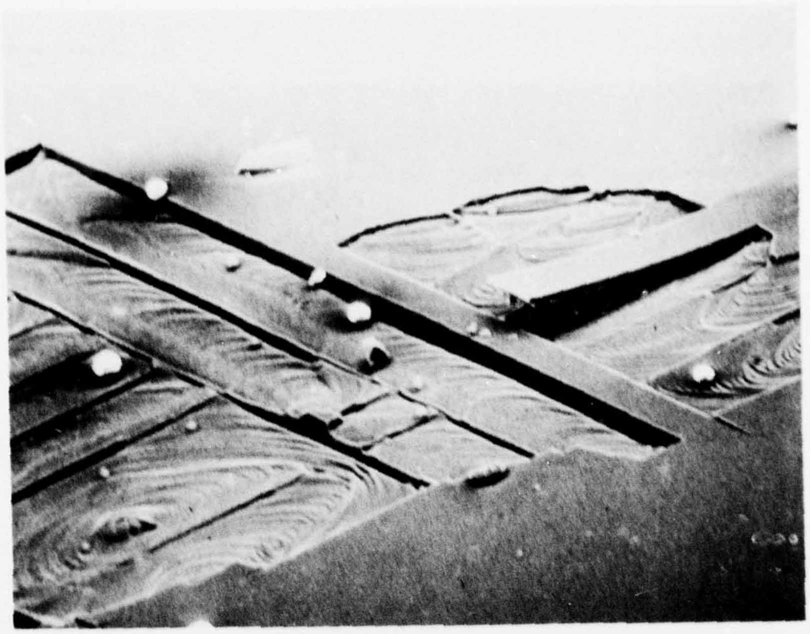

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Figure 4. Silicon Wafer Surface Damage Caused By Nonuniformity in the Pulsed Electron Beam

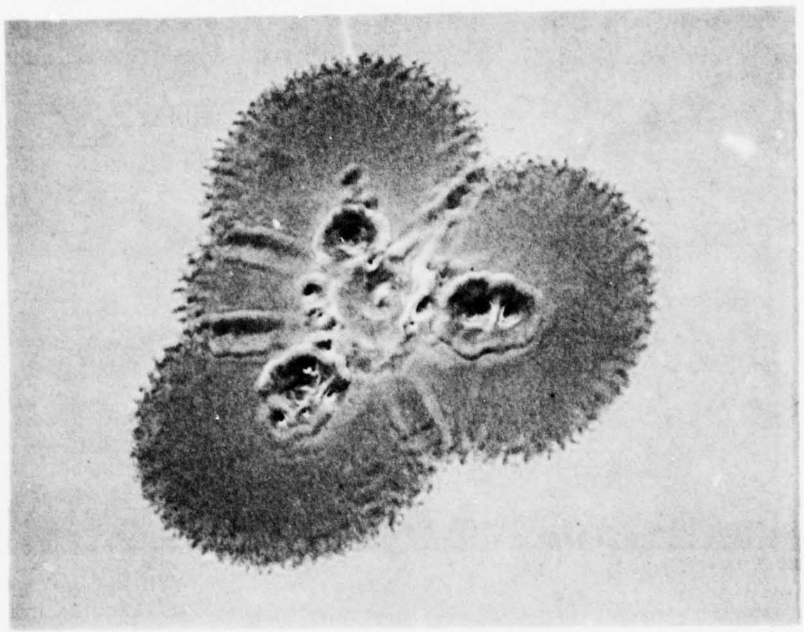

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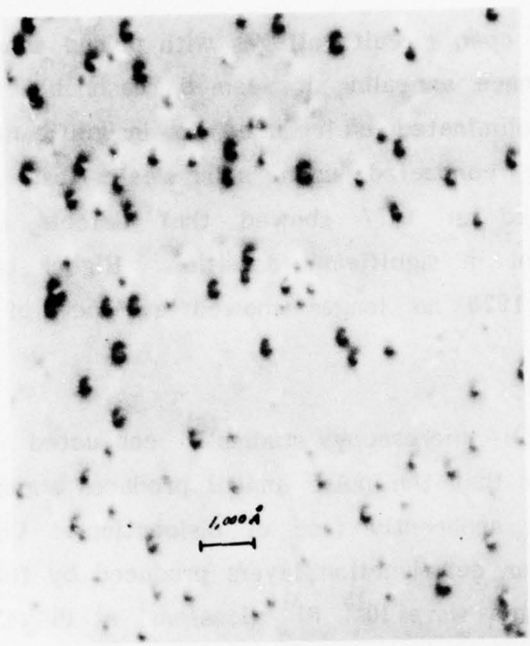
Figure 5. Silicon Wafer Surface Damage Caused by Arcing of the Pulsed Electron Beam

contamination. When cell open circuit voltages with pulsed annealing reached those produced by standard furnace annealing it seemed reasonable to assume that ion contamination had been eliminated or reduced to insignificant levels. Transient capacitance studies were conducted upon solar cell test samples from this program.(4) Samples tested in 1977 showed that defects associated with ion contamination were present in significant densities. Higher performance samples produced and tested in 1978 no longer showed evidence of ion contamination problems.

Transmission electron microscopy studies(5) conducted on electron beam pulse annealed layers show that the pulse anneal produces superb crystal structure junction layers which are apparently free of dislocations. Figure 6 shows TEM views of ion implanted solar cell junction layers produced by furnace annealing and by pulse annealing. Implants were 10^{15} P^{31+} ions/cm^2 at 10 keV into <100> silicon. The furnace annealed material exhibits characteristic dislocations while the pulse annealed material is obviously superior. Other measurements confirm the structural quality of the pulse annealed layers. It is believed that solar cell junctions produced by ion implantation and pulsed annealing now have the potential to have better performance than those by any other presently available method.



A. Thermally Annealed

B. Pulsed Electron Beam Annealed

Figure 6. TEM Photos of Furnace Annealed and Electron Beam Annealed Implanted Layers

SECTION III

PULSED ELECTRON BEAM PROCESSING

3.1 ELECTRON BEAM GENERATION

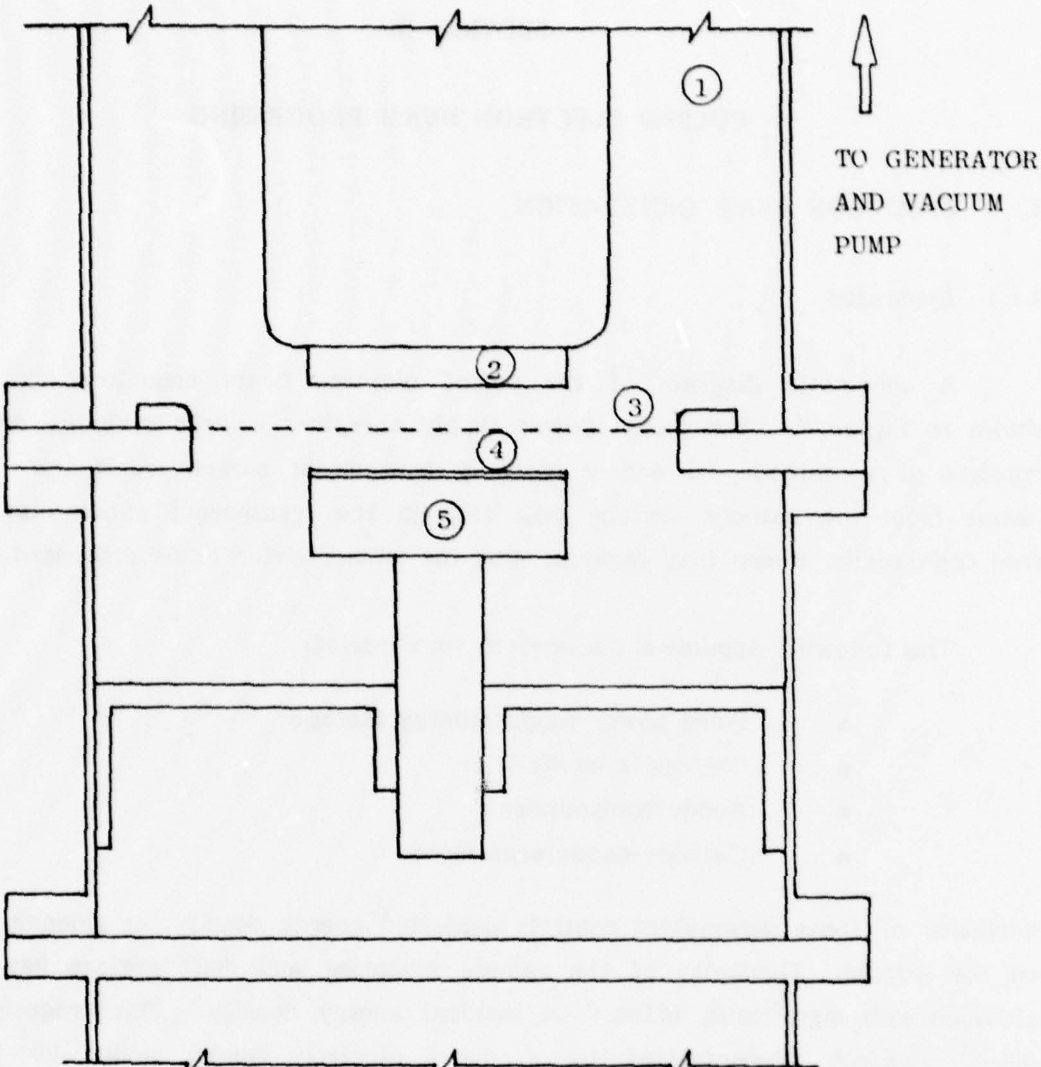
3.1.1 Apparatus

A schematic diagram of the pulsed electron beam annealing apparatus is shown in Figure 7. The pulsed power supply energizes a field emission diode that consists of a cathode (-) and a partially transparent screen anode (+). Electron beams from the cathode surface pass through the transparent anode into a field free drift region where they impinge upon the silicon wafer to be processed.

The following apparatus parameters were varied:

- Pulse power supply energy storage
- Cathode diameter
- Anode transmission
- Cathode-anode separation

Variation of these parameters controls deposited energy density, or *fluence*, incident on the sample. Geometry of the sample mounting and drift regions has smaller, although still significant, effects on incident energy density. This program used a pulsed electron characterized by a mean electron energy under 20 keV and maximum electron energy less than 125 keV. Figure 8 shows the electron energy spectrum for a typical beam used in the annealing experiments. Beam diameters were varied from 3.8 to 7.6 cm depending on the wafer size used. Pulse width (FWHM) was held constant at 0.1 microsecond. Typically, electron beam fluences up to 0.1 cal/cm^2 were used for sintering of contacts and AR coatings and up to 0.5 cal/cm^2 for implant annealing and contact alloying.



1. Vacuum Coaxial Transmission Line
2. Cathode
3. Transparent Anode
4. Sample
5. Sample Holder

Figure 7. Pulsed Electron Beam Generator Schematic Design

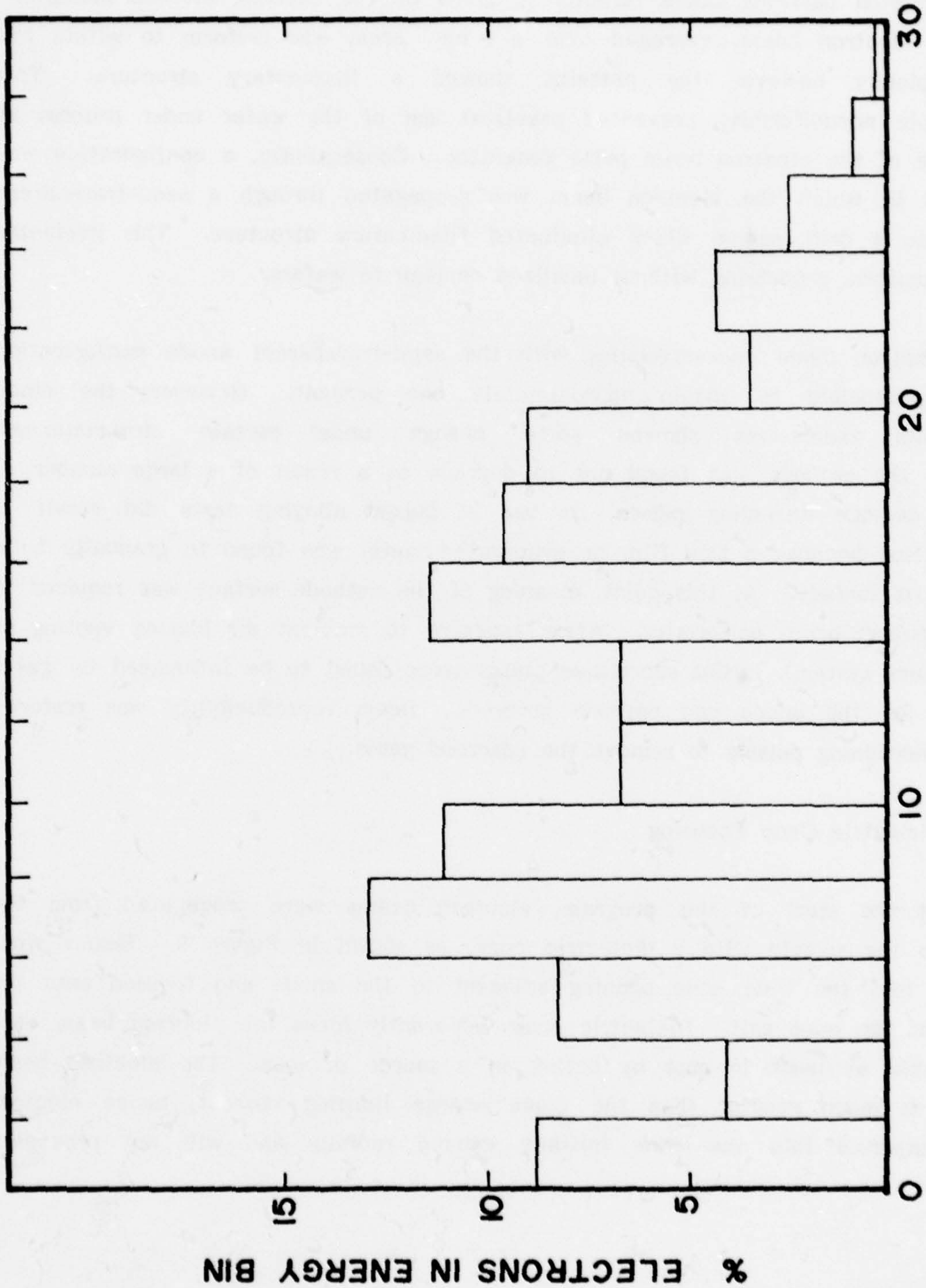


Figure 8. Energy Spectrum of Pulsed Electron Beam

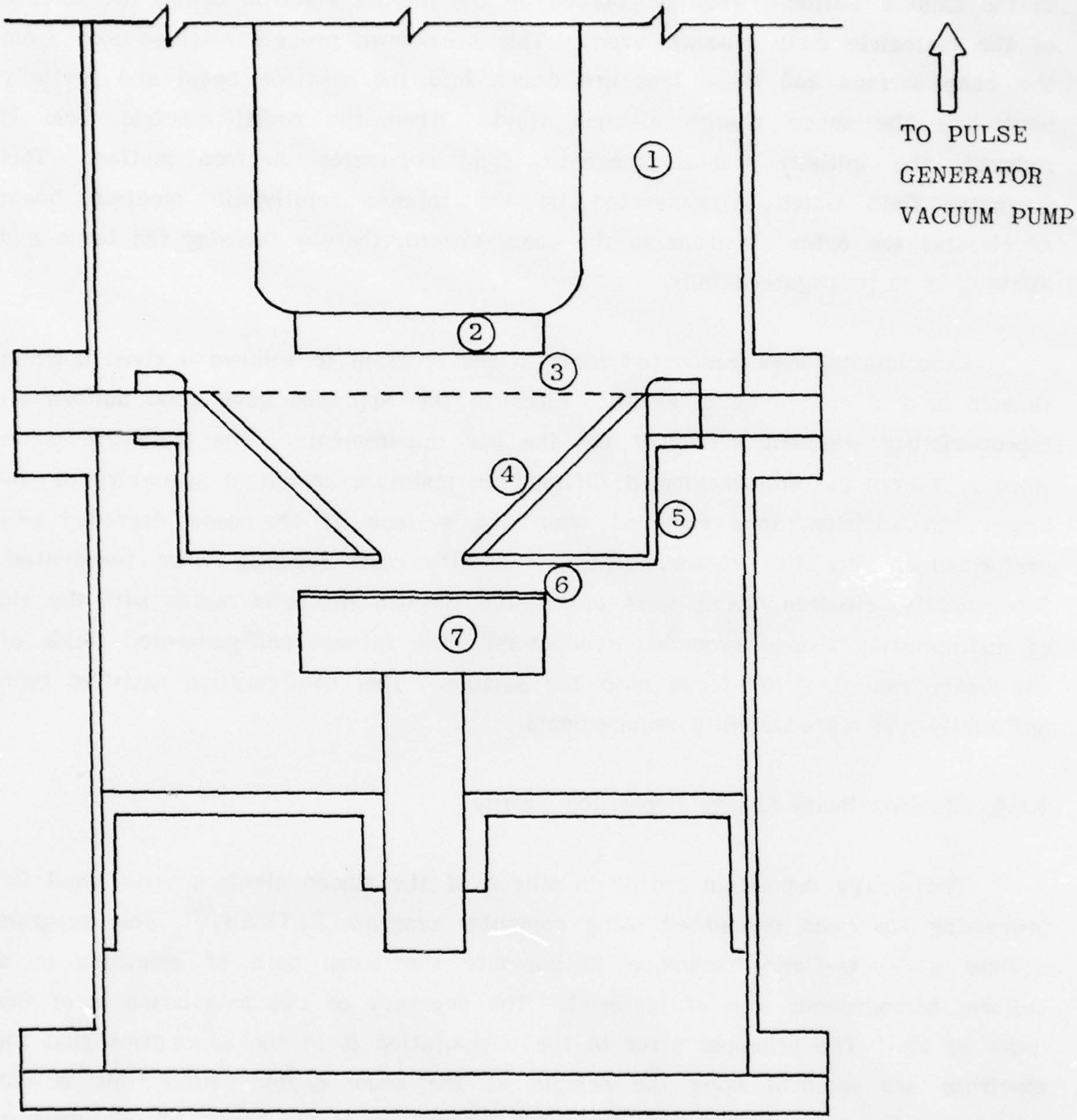
3.1.2 Beam Uniformity and Reproducibility

Emission patterns taken directly in front of the cathode surface indicated that the electron beam, averaged over a 1 cm^2 area, was uniform to within 5%. Microscopically however the patterns showed a filamentary structure. This microscopic nonuniformity prevented practical use of the wafer under process as the anode of the electron beam pulse generator. Consequently, a configuration was employed in which the electron beam was propagated through a semi-transparent anode into a drift region which eliminated filamentary structure. This geometry allowed uniform processing without localized damage to wafers.

Electron beam characteristics with the semi-transparent anode configuration were reproducible to within approximately one percent. However, the diode components themselves showed some change under certain circumstances. Although the cathode was found not to degrade as a result of a large number of implant damage annealing pulses, its use in pulsed alloying tests did result in deterioration because a thin film of evaporated metal was found to gradually build up upon its surface. At this point, cleaning of the cathode surface was required to restore pulsed beam uniformity. After exposure to ambient air (during venting of the vacuum system), initial successive pulses were found to be influenced by gases adsorbed on the anode and cathode surfaces. Beam reproducibility was restored after conditioning pulsing to remove the adsorbed gases.

3.1.3 Dielectric Cone Focusing

At the start of this program, electron beams were progagated from the anode to the sample with a dielectric cone, as shown in Figure 9. Beams were injected into the wide cone opening adjacent to the anode and focused onto the sample at the cone exit. Dielectric cones apparently focus the electron beam onto the sample at least in part by acting as a source of ions. The electron beam current is much greater than the space charge limiting current, hence electron beams injected into the cone initially expand radially and will not propagate



1. Vacuum Transmission Line
2. Cathode
3. Transparent Anode
4. Focussing Guide Cone
5. Cone Holder
6. Sample
7. Sample Holder

Figure 9. Pulsed Electron Beam Focusing with Dielectric Cone

in the axial direction. When bombarded by the intense electron beam, the surface of the dielectric cone "flashes over". This breakdown process releases ions from the cone surface and these ions are drawn into the electron beam and partially neutralize the space charge electric field. When the radial electric field is reduced, the initially weaker magnetic field dominates electron motion. This magnetic field which is generated by the intense relativistic electron beam accelerates the outer electrons in the beam inward, thereby focusing the beam and allowing it to propagate axially.

Experiments were conducted early in the program to achieve a given uniform fluence in a 3 cm diameter circle. Although this approach gave good uniformity, reproducibility was not sufficient for the use requirements. The dielectric cones wore in uneven patterns making it difficult to maintain azimuthal symmetry of the beam. In addition, ions removed from the surface of the cone degraded cell performance. For this reason, experiments with cone focusing were terminated. Subsequently, electron beams were progagated through the drift region with the aid of appropriately shaped grounded conductors. The intense self-generated fields of the beam caused it to focus onto the sample. This configuration satisfied both uniformity and reproducibility requirements.

3.1.4 Electron Beam Energy Deposition Profile

The energy deposition profile in silicon of the pulsed electron beam used for processing has been calculated using computer program ELTRAN.[6] This program utilizes a Monte-Carlo technique to compute the mean path of electrons in a uniform homogeneous slab of material. The accuracy of this calculation is of the order of 5%. The principal error in the computation is in the assumption that all electrons are incident upon the sample at the same angle. While this is not experimentally true, calculations using a single incidence angle of 60 degrees

approximate the measured data quite closely. The calculated energy deposition profile was given in Figure 1. Figure 10 shows results from an experiment conducted to measure the electron beam deposition profile. The beam was drifted through thin aluminum foils into a Faraday cup used to measure collected current. Integrated current is shown as a function of the number of foils penetrated.

Time resolved data exhibits two peaks in the charge deposition profile. The first peak is due to high energy electrons at comparatively low current that are not focused but are absorbed within 5 μm of the surface. Maximum electron energy of this component is less than 125 keV, the threshold energy for electron produced lattice displacement damage in silicon[7]. As the voltage across the diode, and consequently electron energy, decreases, current increases. This gives rise to a second peak. Electrons from this peak are absorbed even closer to the surface. The intense current density of this beam component creates a magnetic field that is sufficient to self-focus the electron beam. Because focusing creates a converging beam, electrons from this component are not incident normal to the surface. This further reduces the electron absorption depth due to increased path length. This self-focused component of the electron beam dominates the measured energy deposition profile.

3.2 THERMODYNAMIC CALCULATIONS

Calculations were performed to compute wafer temperature profile, as a function of depth with time as a parameter, in uniformly irradiated silicon. Some of the deposited energy is conducted away while the remainder locally heats the material. The heat flow equation for this case is:

$$\frac{\partial}{\partial x}\left[K(T)\,\frac{\partial T}{\partial x}\right] + \rho\dot{D} = \rho C_p(T)\,\frac{\partial T}{\partial t} \qquad (1)$$

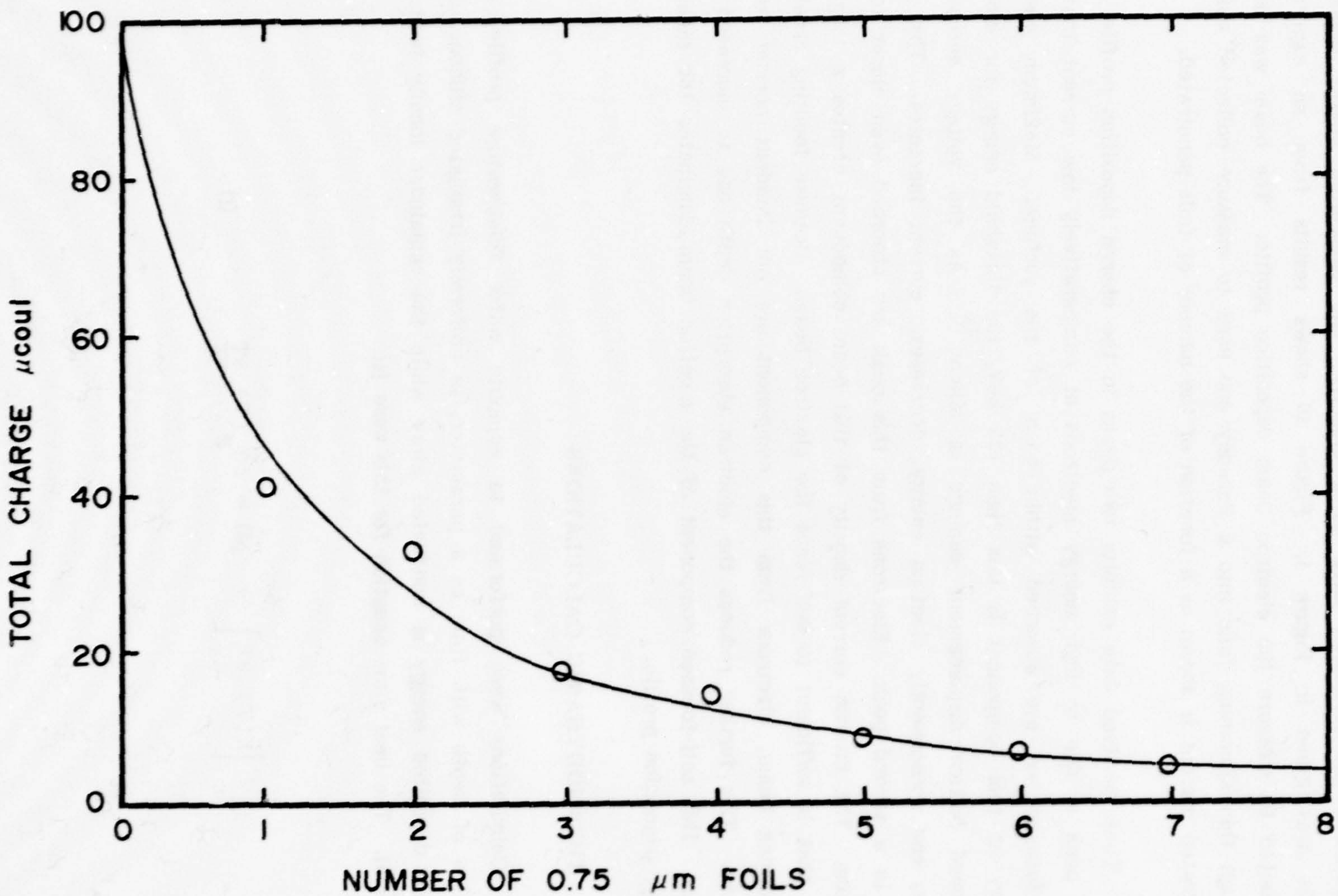


Figure 10. Measured Deposition Profile of Electron Beam: Faraday Cup Integrated Current versus Number of Aluminum Stopping Foils

where:

T = absolute temperature (^{o}K) at the point (x,t)

ρ = density (g/cm^3)

$K(T)$ = temperature dependant thermal conductivity (watts/cm - ^{o}K)

$\rho C_p(T)$ = temperature dependent specific heat (J/cm^3 - ^{o}K)

$D(x,t)$ = rate of energy input from an external source to the point z at time t ($J/sec\text{-}cm^3$)

The boundary conditions are:

1. The material is initially at a uniform temperature T_o

2. The material thickness is large compared to the depth in which energy was deposited, so that:

$$\lim_{x \to \infty} T(x,t) = T_o$$

3. The heat loss at the front surface is given by the radiation power loss per unit area,

$$\varepsilon \sigma T^4$$

Emissivity, ε, of silicon was taken as 0.5 and σ is the Stefan-Boltzmann constant. Corrections to ε with variations in temperature are neglected because the maximum radiated power is very small compared to both the input power and the initial thermal conductivity power loss from the front surface.

Because equation (1) has temperature dependent thermal coefficients, it is non-linear and hence, not amenable to analytic solution. Some simplification is achieved by introducing the new variable:

$$\theta = \frac{1}{K(T_o)} \int_{T_o}^{T} K(T')\, dT' \tag{2}$$

Equation (1) then becomes:

$$\frac{\partial^2 \theta}{\partial x^2} + \frac{\rho \dot{D}}{x(T_o)} = \frac{\rho C_p(T)}{K(T)} \frac{\partial \theta}{\partial t} \tag{3}$$

or equivalently:

$$\frac{\partial \theta}{\partial t} = C^2(\theta) \left[\frac{\partial^2 \theta}{\partial x^2} + \frac{\rho \dot{D}}{K(T_o)} \right] \tag{4}$$

where: $$C^2(\theta) = \frac{K(T(\theta))}{\rho C_p(T(\theta))} \tag{5}$$

is the temperature dependent thermal diffusivity.

The thermal conductivity of crystalline silicon is approximated by the expression[8]:

$$K(T) \sim AT^{-\alpha} \tag{6}$$

Equation (2) then becomes:

$$\theta = \frac{T_o}{\alpha - 1} \left[1 - \left(\frac{T_o}{T} \right)^{\alpha - 1} \right] \tag{7}$$

The thermal diffusivity of crystalline silicon is approximated by the relation:

$$C^2(\theta) = C_o + A_o \theta - B_o \theta^{\gamma} \tag{8}$$

where C_o is the thermal diffusivity at T_o and the constants A_o, B_o and γ are determined by curve fitting to tabulated heat capacity and thermal conductivity data.

Equation (4) is solved numerically by using a spatial mesh of increment Δx and advancing time in steps of Δt. Equation (4) can be rewritten as:

$$\theta(x,t+\Delta t) = \beta(\theta) \left[\theta(x+\Delta x,t)+\theta(x-\Delta x,t)\right]$$
$$+\left[1-2\beta(\theta)\right] \theta(x,t)+\beta(\theta) \frac{\rho\dot{D}(x,t)\Delta x^2}{K(T_o)} \quad (9)$$

where:

$$\beta(\theta) = C^2(\theta) \frac{\Delta t}{\Delta x^2} \quad \text{is evaluated at } \theta(x,t) \quad .$$

Results from a typical calculation were are given in Figure 2. Energy input for this example was taken from the energy deposition of Figure 1. The radiation source was assumed to have a pulse duration of 0.1 μsec and to deposit, at constant power, a total fluence of 0.2 cal/cm^2. The sample was assumed to be single crystal silicon of thickness greater than 40 μm. Δt was set equal to 10^{-10} sec, and x was set equal to 0.5 μm.

At time t = 0 (at the end of the electron beam pulse) sufficient energy has been deposited near the front surface to raise the temperature to the melting point (1410^{o}C). Liquid phase epitaxial regrowth proceeds unidirectionally from within the silicon substrate to the surface. This recrystallization process is very rapid because melting temperatures are maintained for a period only of the order of a microsecond.

Pulsed energy deposition into solids produces large internal stress and pressure waves due to rapid thermal expansion. These effects have been studied in many materials(9) and are believed to be responsible for the surface cracking observed when the pulsed beam fluence significantly exceeds the annealing threshold.

A simple calculation gives approximate values for the expected maximum stress. It is assumed that surface heating causes a stress that tends to bend the crystal and that thermal relaxation of the steep temperature profile relaxes this stress before mechanical equilibrium can be reached. The initial temperature profile can be approximated by:

$$T = T_S(1-x/D)+T_o \quad (10)$$

Here T is the temperature at depth x, T_s is the surface temperature, T_o is room temperature, and D is the depth at which the temperature rise is negligible. The stress at any depth is then set equal to the compressive force, due to thermal expansion, at that depth, plus the tensile force caused by differential expansion of the surrounding material. The resultant stress, S, is given by:

$$S = (C_{11}E_{xx}+C_{12}E_{yy})+C_{44}E_{zz} \tag{11}$$

Here C_{11}, C_{12}, and C_{44} are the elastic constants of silicon and E_{xx}, E_{yy}, and E_{xz} are the strain ratios; Z being taken perpendicular to the slab surface. If E is taken to be proportional to the thermal expansion coefficient, α, Equation (10) becomes:

$$S = (C_{11}+C_{12})\alpha T+C_{44}\alpha T_o \tag{12}$$

Using the values for the strain ratios of silicon at 1000^oC, and ignoring the change in the ratios with temperature, the result is a maximum surface compressive stress of 3.5 kbar and a maximum tensile stress of 1.8 kbar at depth D. For comparison, the yield point of silicon is considered to be approximately 4 kbar.[10]

This relatively crude approximation was checked by a one-dimensional hydrodynamic code, PUFF, that computes stress wave propagation in materials exposed to pulsed radiation sources. An important point in the physics of this code is that the stress parallel to the surface of the slab is derived from the deviatoric stress that is computed from a model for an isotopic medium.[11]

$$\sigma_{11} = -P+S_{11} \tag{13a}$$

$$2S_{11}+S_{\perp} = 0 \tag{13b}$$

σ_{11} is the stress parallel to the surface, P is the pressure, and S_{11} and S are the deviatoric stresses parallel and perpendicular to the surface respectively. The output of the PUFF computation are values of P and S_{11}.

The material is taken to be single crystal silicon and the energy deposition profile is an approximation to that which was shown in Figure 1, using a fluence of 0.16 cal/cm^2. The result indicated that surface spalling would occur. This prediction however is due to the approximation to the deposition profile that is used. The maximum stress perpendicular to the surface is under 10 bars. The estimated stress parallel to the surface exceeds 10^4 bars at a depth of 2.5 μm. While it can be expected that the stress at 2.5 μm is significantly less than the surface stress, this calculation could not output a stress value closer to the surface.

These calculations suggest that thermally induced stresses could be responsible for the surface cracking observed when the beam fluence exceeded the optimum annealing level threshold. The calculations ignore changes in the mechanical properties of silicon due to the amorphous nature of the implanted layer and due to the effects of pre-induced stress.[12] Additional refinement would be needed before the calculations can explain how the energy deposition profile influences annealing and damage thresholds.

3.3 EXPERIMENTAL PULSED ELECTRON BEAM ANNEALING STUDIES

A substantial fraction of total effort under the subject program of this report involved identification of satisfactory pulsed electron beam parameters and procedures for annealing of implanted solar cell junction layers. In order to evaluate changes in electron beam and implantation parameters, open circuit voltage measurements were used as a figure of merit. Open circuit voltage is sensitive to junction quality. Measurements were made at 25°C under AMO illumination with a probe that allowed an examination of the spatial variation of annealing. Values of 545, 580, and 590 mV for 10, 4, and 1 Ω-cm material respectively were selected as pulse process objectives. These values are typical of furnace annealed implanted wafers under the same test conditions.

Implanted ion dose levels used for solar cell junction purposes are sufficiently high that the implanted layer was made amorphous and of high electrical resistivity. Annealing restores the crystal structure and causes electrical activation. After implant, the amorphous silicon surface exhibits a subtle, uniform change in visual appearance. Proper furnace annealing uniformly restores the crystalline silicon surface character. A silicon wafer subjected to pulsed annealing exhibits a signature of the annealing beam. Figure 11 shows a 3-inch diameter implanted silicon wafer subjected to an electron beam annealing pulse of diameter somewhat less than 3 inches. Although the pulse annealed region can exhibit excellent crystallinity using a wide range of pulse parameters, good junction performance requires optimized conditions.

It is observed that excellent structural restoration of implant damaged silicon crystal is produced by a range of electron beam pulse conditions. Figure 12 shows helium ion backscattering measurement results from implanted silicon without annealing, with good thermal annealing in a furnace, and with pulsed electron beam annealing.[13] Implants were 3×10^{15} P^{31+} ions/cm^2 at 10 keV into $\langle 100 \rangle$ wafers. Ion backscattering from the unannealed material shows the implanted region to be amorphous. After furnace annealing, crystalline structure is seen to be restored, but not completely. Furnace annealing typically results in formation of polycrystallites within the implanted layer. The backscattering profile from the pulsed electron beam annealed layer shows virtually complete restoration of virgin silicon crystal quality.

3.3.1 Electron Beam Fluence Effects

Although a range of electron beam parameters would result in restoration of the implanted silicon crystal structure, junction quality was found to depend upon a number of factors. In particular, it was observed that with the laboratory electron beam pulse facility employed, junction open circuit voltage generally increased with increasing beam fluence. Maximum V_{oc} values were achieved at beam fluence

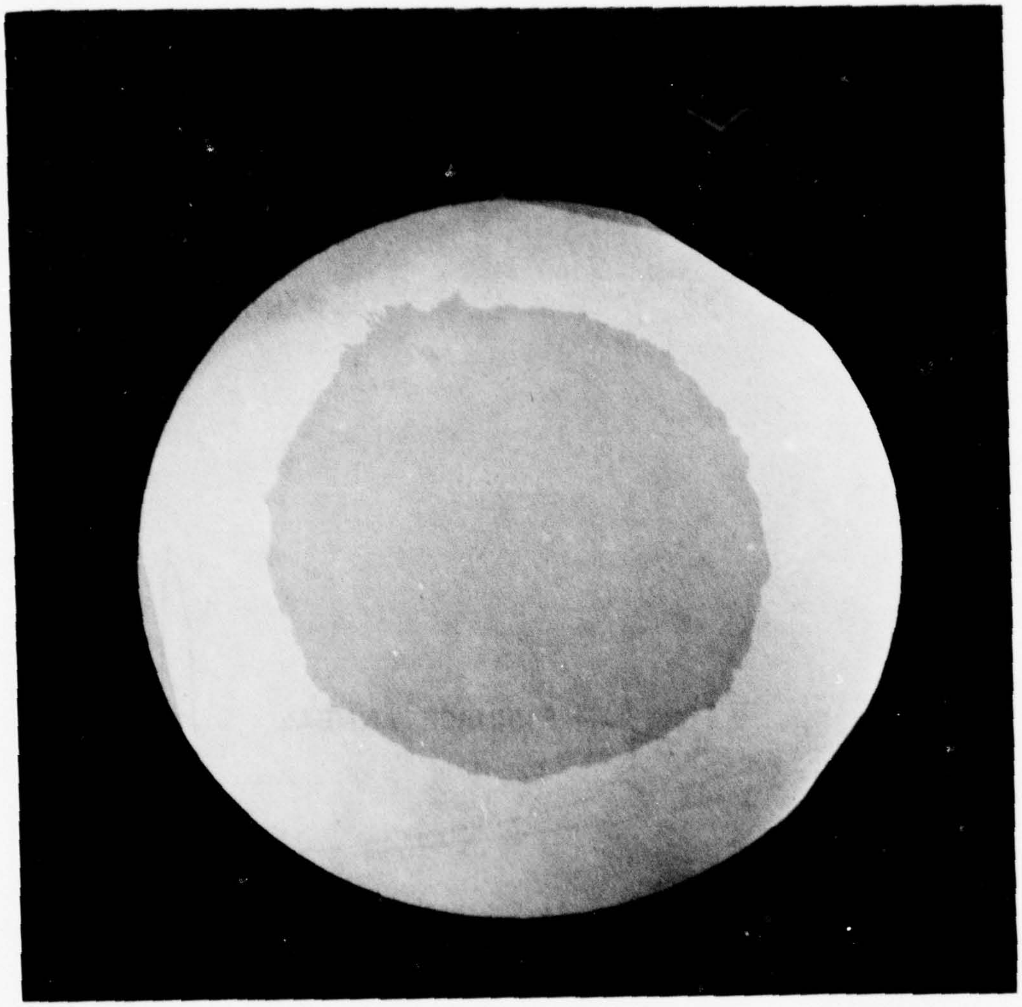


Figure 11. 3-inch Diameter Implanted Silicon Wafer Exhibiting Pulsed Electron Beam Anneal Signature

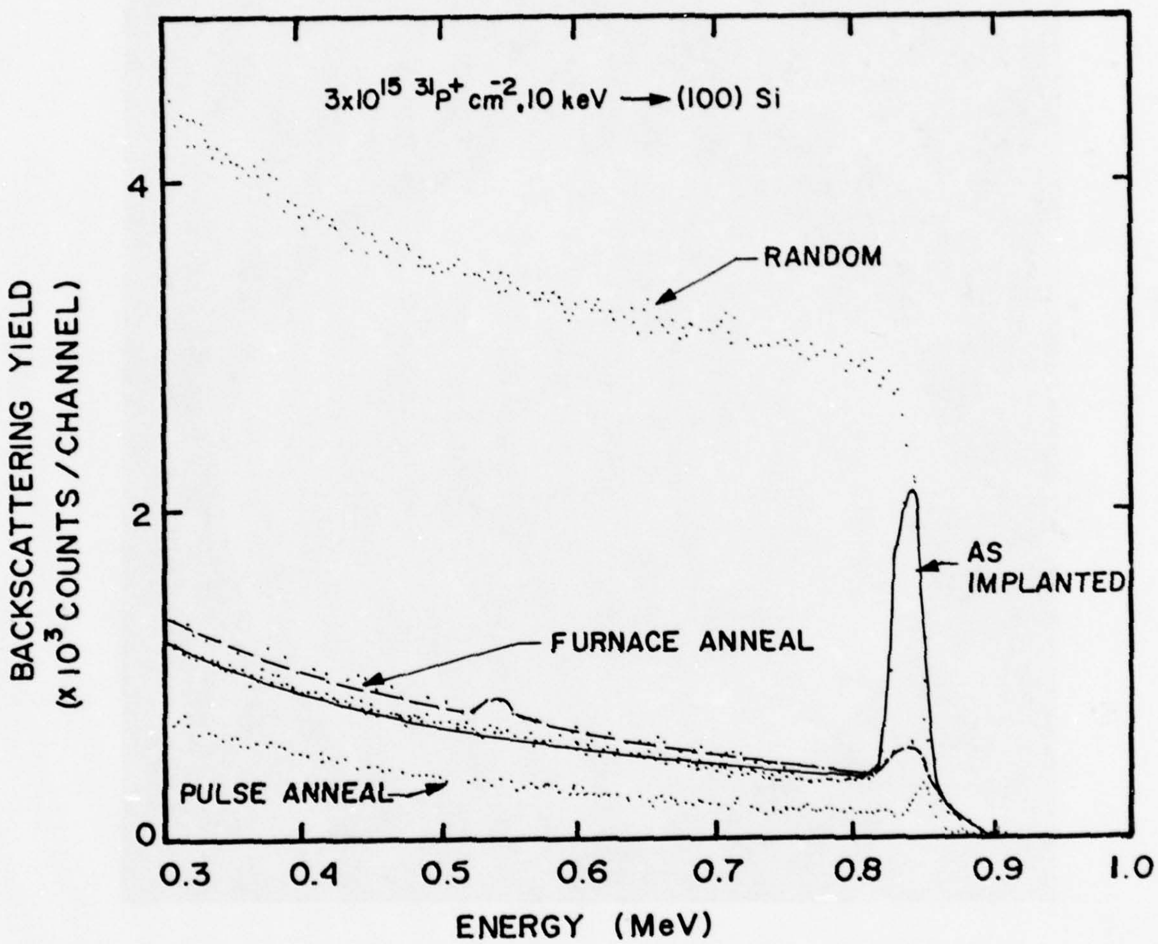


Figure 12. Helium Ion Backscattering from Furnace and Electron Beam Annealed Implanted Wafers

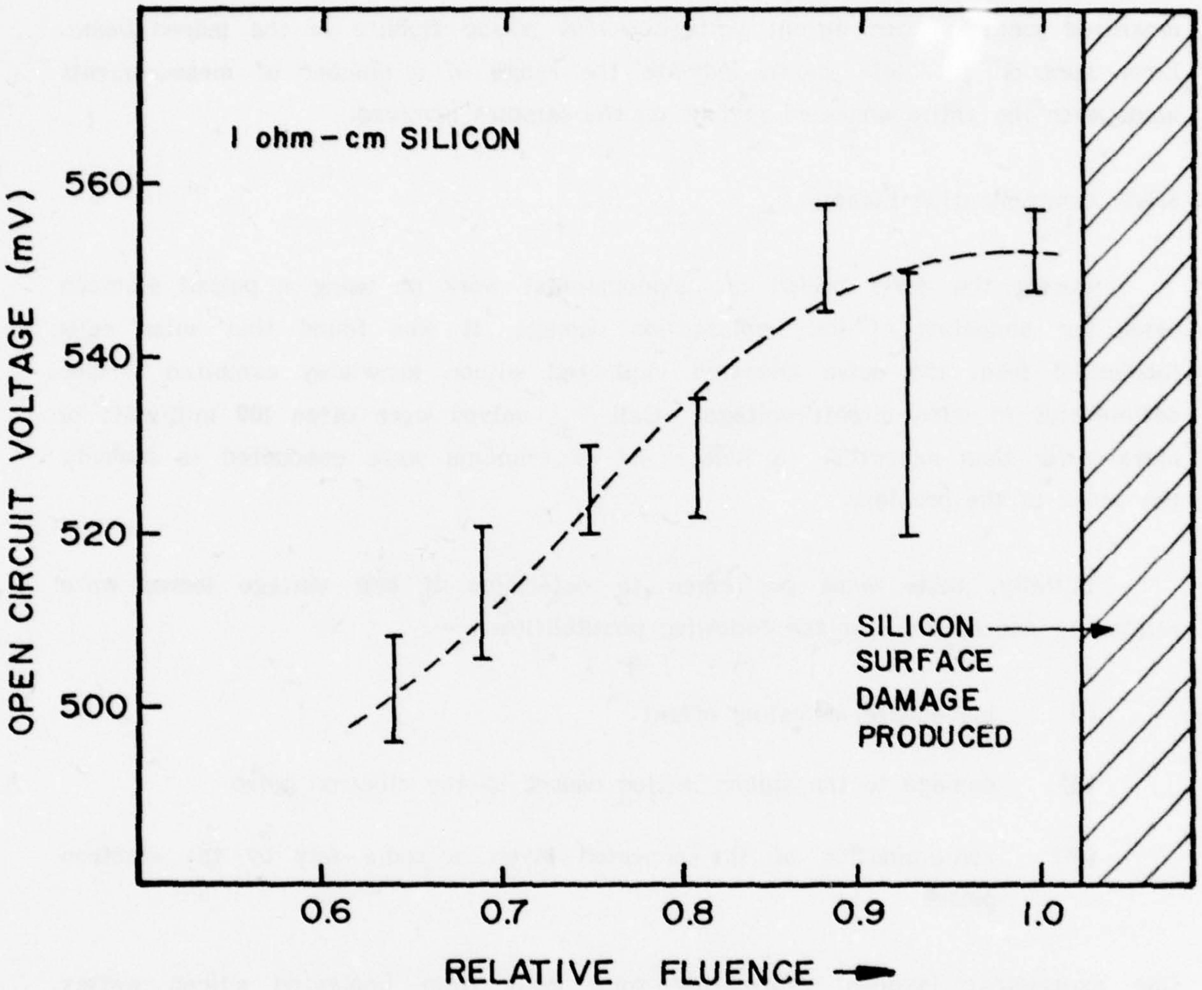


Figure 13. Junction Open Circuit Voltage Versus Fluence

levels which approached the threshold for creation of surface damage to the wafer. Figure 13 presents results from a particular test employing 1 ohm-cm silicon wafers implanted with 5 x 10^{15} P^{31+} ions/cm^2 at 10 keV. Data shown is measured junction open circuit voltage versus pulsed fluence in the pulsed beam. Error bars on the data shown indicate the range of a number of measurements made over the entire annealed regions on the samples involved.

3.3.2 Contamination Effects

During the early period of developmental work on using a pulsed electron beam for annealing of ion implantation damage, it was found that solar cells fabricated from the pulse annealed implanted silicon invariably exhibited serious deficiencies in open circuit voltage. Cell V_{oc} valves were often 100 millivolts or more lower than expected. A number of experiments were conducted to identify the cause of the problem.

Initially, tests were performed to determine if cell voltage losses were related to one or more of the following possibilities:

(i) inadequate annealing effect

(ii) damage to the silicon lattice caused by the electron pulse

(iii) contamination of the annealed layer in some way by the electron pulse.

One experiment involved fabricating solar cells from implanted silicon wafers subjected to three different sets of anneal processing:

(1) furnace anneal

(2) pulsed electron beam anneal followed by furnace anneal

(3) furnace anneal followed by pulsed electron beam anneal.

Cells fabricated from wafers subjected only to furnace annealing exhibited normal open circuit voltages. Cells processed from wafers subjected to pulsed annealing either before or after furnace anneal were characterized by low open circuit voltage values. This observation demonstrated that the low V_{oc} values were not the result of an inadequate annealing effect by the pulsed electron beam but rather were caused by the beam itself.

It remained to be determined whether the problem caused by the electron beam involved damage to the silicon lattice or contamination of the annealed material. No damage effects could be visually identified after proper pulse conditions. Tests were conducted in which a magnetic field was used to deflect away the electron beam before it could impact upon samples in position for normal pulsed annealing. Ionic contaminants, if they were present in the electron beam, because of their mass would undergo much less deflection and could still reach the normal sample anneal position. Implanted silicon wafers were pulsed in this system. No annealing effect took place. However, solar cells fabricated using furnace anneal before or after exposure to the deflected pulse residue continued to exhibit reduced open circuit voltages. Contamination was established as the cause of low open circuit voltages.

At the time the experiments discussed above were conducted, the electron beam pulse generator consisted of a graphite cathode, a fine tungsten mesh anode and a beam guide cone of lucite or quartz. The possible sources of ionic contamination were considered to be:

(i) the cathode surface

(ii) the anode screen surface

(iii) the guide cone surface

(iv) residual gas in the pulse generator vacuum chamber.

It was found that elimination of the guide cone from the pulse generator immediately resulted in improved open circuit voltages of pulse annealed cells. However, the open circuit voltages of pulse annealed junctions continued to remain up to perhaps 30 millivolts lower than values from similar furnace annealed implanted junctions. Table 1 compares pulse annealed and furnace annealed implanted phosphorus junction cell open circuit voltages under AM0 illumination at 25°C. Cells indicated were simple N^+/P structures without back surface fields.

After correction of gross contamination originating from the guide cone surface, the remaining minor deficiencies in pulse annealed junction voltages were suspected to also be associated with ionic contamination. Tests were conducted using different cathode and anode materials, but junction open circuit voltages did not increase. Vacuum in the pulse generator was generally of the order of 10^{-4} Torr. Higher V_{oc} values did not result when pulsing was conducted under 10^{-6} Torr vacuum. A corrective action which would raise pulse annealed junction voltages to full objective levels was not identified. Because voltage losses were minor, specific efforts on this task were eventually abandoned in favor of process development work needed to achieve high efficiency ion implanted cell structures.

Late in this program, transient capacitance measurement techniques being utilized by Air Force personnel at Rome Air Development Center, Hanscom AFB, MA were recognized to offer possibilities for examining certain charcteristics of pulsed electron beam annealed junctions. Samples were submitted to RADC by AFAPL in 1977 and again in 1978. Defects identified as probably associated with contaminant carbon atoms were observed in the depletion regions of pulse annealed junctions of the 1977 samples. These defects were no longer present in the 1978 samples.(4)

By the time the 1978 transient capacitance study samples had been fabricated, junction open circuit voltage shortages had ceased to be a problem of concern. The problem had not been specifically solved but rather had disappeared without particular notice. A graphite cathode continued to be used in the pulse generator. However, wafer cleaning and handling techniques had significantly

TABLE 1

Comparison of Pulse Annealed and Furnace Annealed Implanted Junction Cell Open Circuit Voltages

Silicon Resistivity (ohm-cm)	Cell V_{oc} (Millivolts)	
	Achieved by Pulse Anneal	Typical of Furnace Anneal
10	555	550
4	583	585
1	591	600
0.1	570	600

AMO 25°C

N^+/P Cells 2x2cm

improved during the period and a cryogenic baffle had been added to the electron beam pulse generator diffusion pump. It is now believed that carbon found in the junction region and the minor reductions of junction V_{oc} observed in the 1977 samples were associated with rapid diffusion of surface contaminants into the junction layer during the transient liquid state step of the pulse anneal process. The contaminants involved would have been residues from processing and handling and condensed hydrocarbons originating from the diffusion pump of the pulse generator.

3.3.3 Pulse Anneal Process Depth

Under this program the pulsed electron beam annealing process was developed for application to high efficiency silicon solar cells. Implantation parameters were directed toward achieving very shallow junctions. Pulsed electron beam parameters described in Section 2 and 3.1 above were selected for annealing of low energy phosphorus ion implants.

Table 2 summarizes the results of one experiment to examine the effect of particular pulsed electron beam parameters upon phosphorus ion implants of different energies. All implants were 10^{15} P^{31+} ions/cm^2 into <100> silicon at 7^o off normal. Based upon observed open circuit voltages from the pulse annealed junctions, depth of satisfactory annealing with the particular electron beam utilized in this case was only about 0.1 μm.

Electron beam parameters used for most of the developmental program were such that implants to a depth of approximately 0.3 μm could be properly annealed. This apparently meant that depth of melting caused by the pulse was approximately 0.3 μm. Within silicon at melt temperature, diffusion coefficients of dopant species can be many orders of magnitude higher than in silicon at temperatures just below melt.(14) Implanted dopant was found to redistribute to approximately the depth melted. Consequently, even the lowest energy implants resulted in junction depths of approximately 0.3 μm after pulse annealing.

3.3.4 Effects of Wafer Resistivity

The pulsed electron beam generator has a low impedance diode. To the electron beam incident upon its surface, an implanted silicon wafer appears as a capacitor to ground in parallel with an inductor and resistor in series. Very large momentary currents are involved in the anneal process and the wafer being pulsed becomes an active circuit element with some influence upon the beam parameters. Wafers of different base resistivities can have sufficiently different effective resistance to influence the beam parameters. As a result, separate optimized electron beam pulse parameters were developed and subsequently utilized for 10, 4, 1 and 0.1 ohm-cm silicon.

TABLE 2

Junction V_{OC} Dependence on Implant Energy for Fixed Pulse Electron Beam Parameters

Implant Energy (keV)	Implanted Dopant Depth (μ m)	Pulse Annealed Junction V_{oc} (mV at 25°C, AM0)
100	0.63	426 - 470
25	0.28	498 - 504
20	0.18	517 - 529
15	0.15	516 - 531
10	0.12	512 - 520
5	0.10	530 - 537

Implants: 10^{15} P^{31+} ions/cm^2 at 7^o

Silicon : <100> 10 ohm-cm CG

3.4 PULSED ELECTRON BEAM ALLOYING

The primary application of pulsed electron beams under the program was for annealing of ion implantation damage. However, some consideration was also given to pulsed electron beam treatments of metal films to produce ohmic contact interface with the silicon. Demonstration was performed with aluminum but other contact materials could have been used. Pulse alloyed aluminum on the back surface of a N^+/P structure was found to produce an N^+/PP^+ cell exhibiting back surface field effect.

The pulsed electron beams used for alloying experiments were of appreciably higher fluence than those used for implant damage annealing. In order to produce the desired effect it was necessary to elevate the silicon-aluminum interface to above the 577°C required for eutectic formation. Simple experiments were performed without any effort to select particular temperature ranges for the interface. Films of between 100Å and something less than 1000Å were effectively pulse treated. Thicker 5 μm films peeled off when pulsed with no interaction between the silicon and aluminum.

Figure 14 shows a silicon wafer with 200A aluminum film after the electron beam alloying pulse. Pulsing was conducted at approximately 10^{-4} Torr and the entire aluminum film was momentarily heated to well above its melting temperature. In addition to alloying with the silicon, some surface oxide was found to form on the aluminum surface due to high temperature reaction with residual oxygen. Pulse alloyed layers were found to provide low resistance ohmic contact and could be an excellent base for contact bulk subsequently deposited over top.

A test was conducted to determine if pulse alloyed aluminum films could provide back surface field effect. Aluminum layers 100Å thick were evaporated onto 4 ohm-cm silicon wafer back surfaces. Five wafers were furnace processed at 650° for 15 minutes while five others were pulsed to form the aluminum-silicon alloy. Junction implants were introduced into the wafers and pulsed electron beam annealing was used to remove the implant damage. Contacts were applied and open circuit voltages at 25°C under AM0 illumination were measured. Results are

Figure 14. Silicon Wafer with Pulse Alloyed Aluminum Film

listed in Table 3. The open circuit voltages from the wafers which had been furnace alloyed were significantly lower than those which were pulse alloyed. The difference is believed to be due to back surface high-low junction effect. No optimization of this processing was attempted.

TABLE 3

Comparison of Open Circuit Voltages from Cell Wafers
With Furnace and Pulse Alloyed Aluminum Backs

Wafer No.	Back Surface Aluminum Film Treatment	Open Circuit Voltage Millivolts)
1	650°C-15 minutes in furnace	485 - 505
2		525 - 535
3		545 - 555
4		530 - 540
5		530 - 540
6	Electron beam pulsed	555 - 570
7		550 - 570
8		555 - 575
9		550 - 575
10		540 - 565

Silicon: 4 ohm-cm CG <111>
Pulse annealed implanted junctions

AM0 at 25°C

SECTION IV

SOLAR CELL PROCESSING

4.1 GENERAL

At the start of this program, device structural refinements utilized in diffused junction "violet" and nonreflecting surface silicon solar cells had not been incorporated into ion implanted cells. Development had not been previously initiated to allow ion implanted cells to be fabricated with efficiencies appreciably beyond 11% AM0. Under this program, investigations were to be performed to identify necessary advances in the detailed structure of the ion implanted silicon solar cell. After structural requirements had been determined, development was then to emphasize utilization of pulsed electron beam processing toward further optimization of cell performance. Relative to diffusion, ion implantation involves distinct differences in device structures which can or should be fabricated. The implanted dopant profile shape, peak concentration and junction depth all are of serious concern in developing the cell. The procedures used for implant damage annealing, whether furnace or pulse process, have important effects upon output character of the cell.

In order to substantially improve the performance of ion implanted silicon cells, the entire cell structure had to be considered. The implanted junction was of course critical, but procedures were necessary also for implantation of a back surface field layer. Satisfactory contacts and antireflective coating were required. Silicon growth method, orientation, and resistivity had to be selected. Implantation of junctions into texturized surface material was examined. Finally, total processing sequences for implanted cells were tested.

Optimization of ion implanted silicon cells was not completed under the program. A number of developmental activities to further improve the cell structure remain to be conducted at some future time. However, even without optimization, relatively simple implanted 2 x 2cm cells with efficiencies above 13.5% AM0 were produced.

4.2 SOLAR CELL STRUCTURE

4.2.1 Ion Implanted Junctions

In the ion implantation process, energetic ions impact upon the solar cell wafer surface and lose energy by Coulomb interactions with atoms of the wafer as they penetrate. Analytical predictions of ion stopping are usually based on LSS theory.(15,16) The stopping distribution of monoenergetic ions is essentially Gaussian. In the absence of channeling effects which will be mentioned below, the profile of the implanted dopant before annealing is given by:

$$n(x) = \frac{Q}{\sigma \sqrt{2\pi}} \exp - (x-Rp)^2/2\sigma^2$$

where: $n(x)$ = implanted ion concentration at depth x

Q = ion influence

R_p = projected ion range

σ = projected range standard deviation

Figure 15 illustrates predicted distribution profiles for 10^{15} cm^{-2} fluences of 10, 40 and 100keV P^{31+} ions in silicon. These predicted stopping distributions are actually valid only for implantation into amorphous targets. In the case of crystalline targets such as the silicon wafer, ions can "channel" along aligned directions in the crystal lattice. An ion aligned with an axis direction can make fewer interactions and as a result will penetrate more deeply than predicted. Standard procedure is to intentionally misalign the ion beam and the wafer surface. This is performed automatically within most implanter end stations. However, because ions undergo small angle scattering as they penetrate and interact with the substrate, some can be scattered into aligned axis paths. These then produce a "tail" on the predicted dopant profile. Phosphorus has a particularly strong tendency to exhibit this effect.

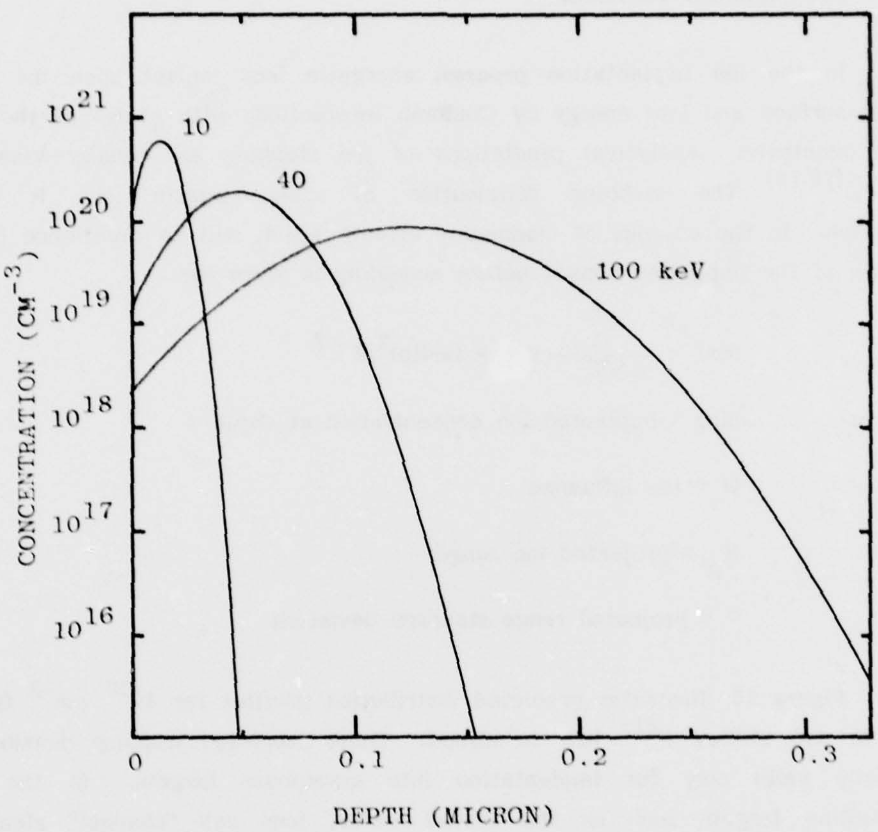


Figure 15. Predicted Profiles in Silicon for 10^{15} cm^{-2} Fluences of 10, 40, and 100 keV P^{31+}

Figure 16 shows an experimentally measured profile in silicon for a 25 keV phosphorus implant after damage anneal at $750^{o}C$ for 30 minutes. The deep tail due to channeling is apparent. The measurement was made by successive anodic oxidation layer stripping and 4-point probing.

For solar cell purposes, it is desired that the implanted junction be shallow. The implant should also provide sufficiently low junction layer sheet resistance to allow cell series resistance to be kept satisfactorily low. Table 4 lists measured junction depths and measured sheet resistances for a series of low energy phosphorus implants into 10 ohm-cm $\langle 100 \rangle$ CG silicon. Implant anneals were performed at $750^{o}C$ for 30 minutes. Measured junction depths shown in Table 4 are, except for the case of 5 keV implant, deeper than desirable for very high efficiency cells. The shapes of the dopant profiles produced also present significant problems in achieving high cell performance. As can be seen in the experimental profile of Figure 16 or in the predicted profiles of Figure 15, the peak concentration of implanted dopant falls below the silicon surface. In this situation a drift field results in the layer from the surface to the concentration peak which accelerates minority carriers toward the surface, i.e., away from the junction. The region is effectively a dead layer. It would be desirable to be able to perform junction implants in which the junction layer is very shallow, say 0.15 μm or less, and the dopant distribution declines monotonically from the silicon surface.

One obvious possibility for producing adequately shallow junctions with desirable profile shape is to perform the implant through a surface oxide. After implant, and perhaps implant damage anneal, the oxide can be removed. The result should be a shallower junction and, with correct oxide thickness, resulting dopant concentration peak at the silicon surface. Under the program, appreciable work was performed on this particular approach to implanted junction processing. Results were generally unsuccessful in that solar cells fabricated using this approach to junction implantation never exhibited better response characteristics than similar cells prepared by simple direct implant.

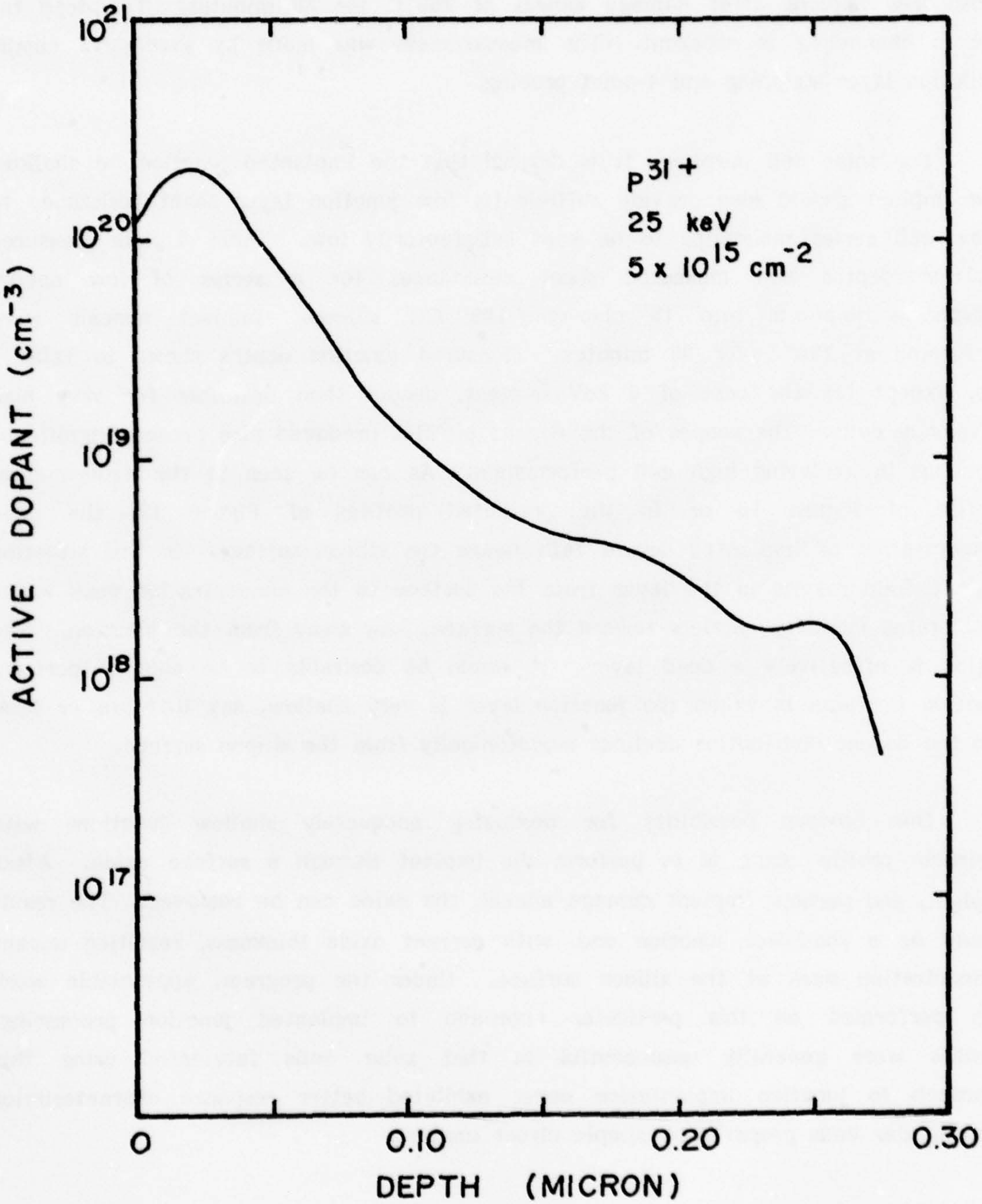


Figure 16. Experimentally Measured Profile

TABLE 4

Measured Parameters - Shallow Junction Implants

Implant Energy (keV)	Fluence (ions/cm^2)	Implant Angle	Sheet Resistance ($\Omega/\Box$)	Junction Depth (μm)	
				Measured	Predicted
25	10^{15}	15°	126	0.32	0.11
20	10^{15}	15	142	0.29	0.09
15	10^{15}	15	149	0.27	0.06
10	10^{15}	15	171	0.22	0.05
5	10^{15}	15	315	0.14	0.03
25	2×10^{14}	7°	450	0.30	0.11
20	2×10^{14}	7	563	0.28	0.09
15	2×10^{14}	7	594	0.24	0.06
10	2×10^{14}	7	684	0.20	0.05
5	2×10^{14}	7	1058	0.14	0.03

The problem with implantation through an oxide or other surface coating involves recoil of atoms from the surface layer into the substrate. Collisions of high energy ions with the surface atoms cause surface atoms to become "knock-on" recoils to penetrate and contaminate the substrate surface. The degree of this effect is not trivial, the number of oxygen recoil atoms entering the substrate can be many per incident ion if the surface oxide has thickness comparable to projected ion range.(17) Oxygen atom recoils result in significant residual damage in the silicon after annealing.(18) High recoil atom concentrations result from implants through any surface coating. In general, these can seriously degrade the surface region silicon below the coating and reduce the contribution that the region might otherwise make to cell output performance.

Other possibilities for reducing junction depth and correcting the implant distribution profile were examined. These involved formation of a surface oxide after the implant then removing the oxide with hydrofluoric acid. Furnace anneals were performed in atmosphere containing oxygen or anodic oxidation of the wafer surface was employed after implant anneal. Improvements in cell blue response were sometimes observed, but generally it was found that thickness removal requirements were critical to a degree which prevented satisfactory process control. These procedures were consequently not adopted for cell fabrication purposes.

Problems associated with developing high performance shallow junctions were not completely resolved under this program. However it was found that if the implanted dopant profile shape can be adjusted to have highest concentration essentially at the silicon surface, good cell performance can be achieved even with 0.25 - 0.30 μm junction depth. In the case of device structural development performed using furnace annealing, sufficiently high temperatures to allow dopant diffusion during annealing were required. Figure 17 shows expected effect of 30 minute 800°C or 900°C furnace anneals on the predicted basic distribution of phosphorus resulting from a 5 keV implant. Experimentally it was found that a 5 or 10 keV phosphorus implant combined with furnace annealing involving 15 minutes at 850°C provides a satisfactory profile shape with a junction depth of 0.25 to 0.30 μm.

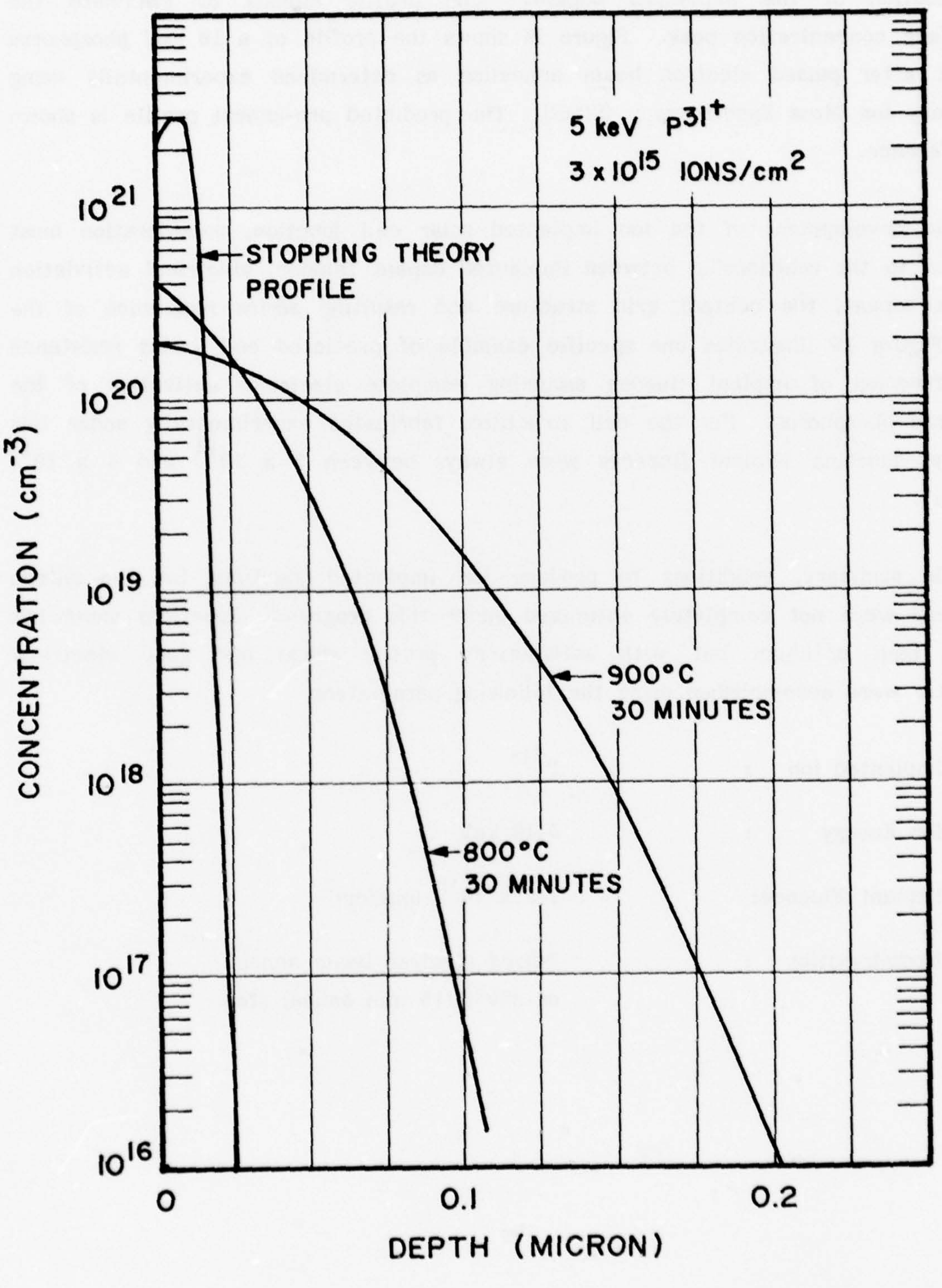


Figure 17. Predicted Effect of Diffusion During Furnace Annealing of Implanted Phosphorus

The use of pulsed electron beam annealing involves extremely rapid redistribution of the implanted dopant. The profile adjusts to eliminate the *subsurface concentration peak.* Figure 18 shows the profile of a 10 keV phosphorus implant after pulsed electron beam annealing as determined experimentally using Secondary Ion Mass Spectroscopy (SIMS). The predicted pre-anneal profile is shown for reference.

In development of the ion implanted solar cell junction, consideration must be given to the relationship between implanted dopant fluence, electrical activiation of this dopant, the contact grid structure and resulting series resistance of the cell. Figure 19 illustrates one specific example of predicted cell series resistance as a function of implant fluence assuming complete electrical activation of the implanted phosphorus. For the cell structures fabricated experimentally under this program, junction implant fluences were always between 5×10^{14} and 5×10^{15} ions/cm^2.

In summary, conditions to produce ion implanted junctions for the silicon solar cell were not completely optimized under this program. Junctions somewhat deeper than optimum but with satisfactory profile shape and good electrical character were accomplished using the following parameters:

Implanted Ion	:	P^{31+}
Ion Energy	:	5-10 keV
Implant Fluence:		$1\text{-}5 \times 10^{15}$ ions/cm^2
Redistribution	:	Pulsed electron beam anneal or 850°C/15 min anneal step

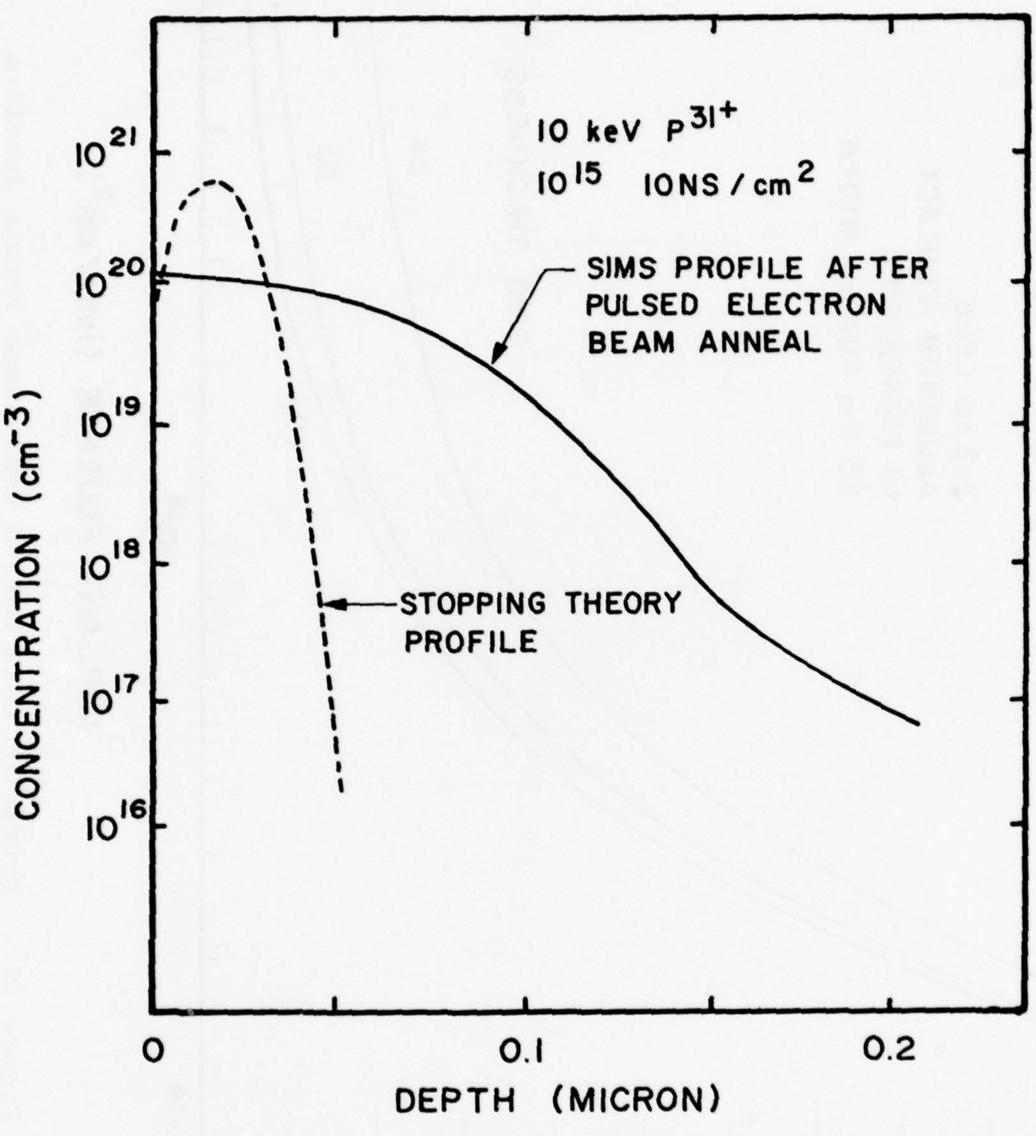


Figure 18. The Effect of Pulsed Electron Beam Annealing on the Profile of Implanted Phosphorus

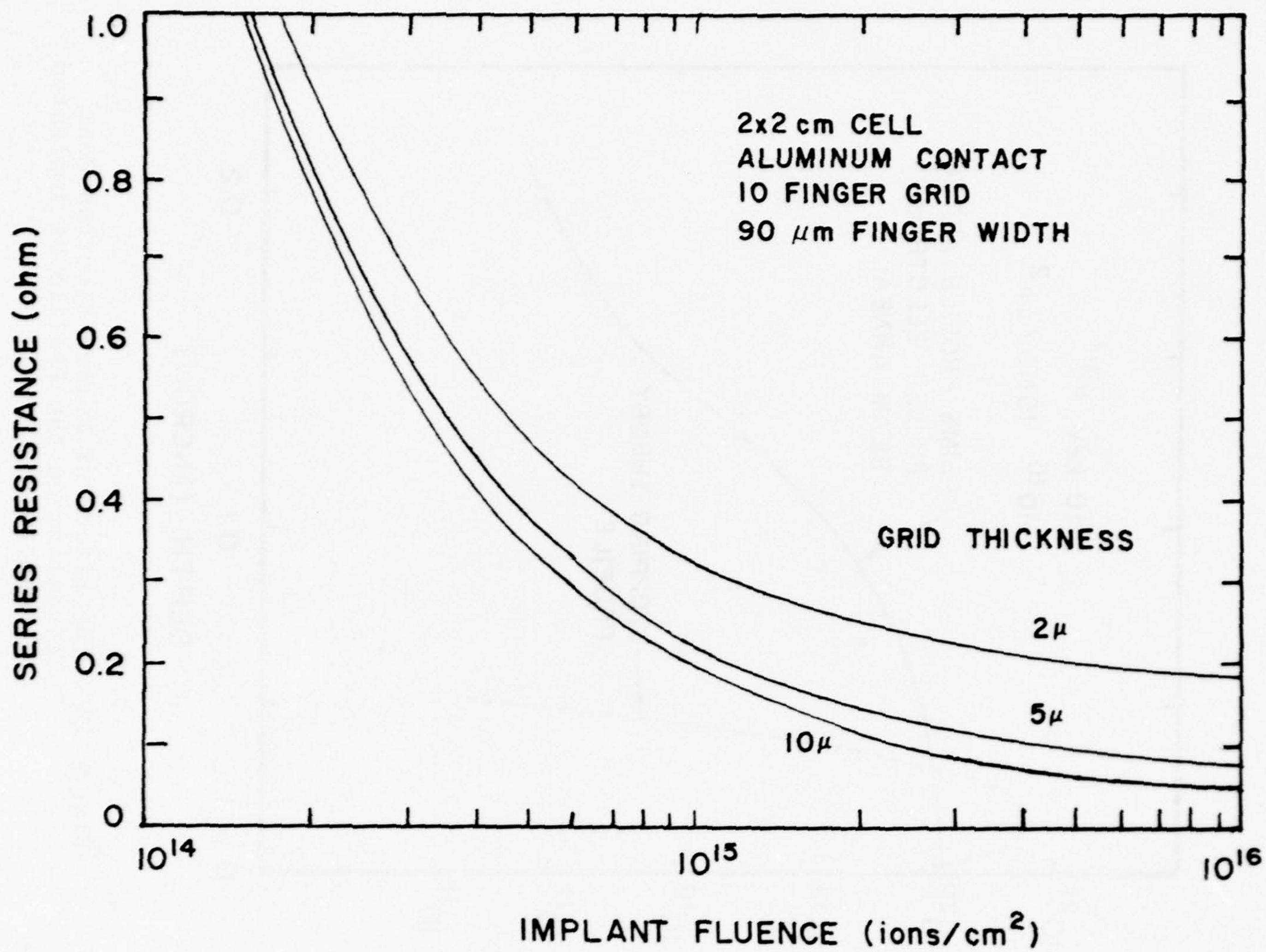


Figure 19. Predicted Cell Series Resistance versus Junction Implant Fluence

4.2.2 Back Surface Doping

In order to produce a high performance N^+/PP^+ cell structure, the back surface P^+ layer should provide the following:

(i) An ohmic contact underlayer.

(ii) Voltage enhancement due to high-low junction behavior.[19]

(iii) Current enhancement due to photon reflection and reduced carrier recombination.

The ohmic contact underlayer is easily accomplished by any of a number of possible approaches which produce heavy P^+ doping in the silicon immediately adjacent to the cell back contact. Cell voltage and current enhancement effects generally associated with a back surface field are more difficult to achieve.

The most effective procedure presently available for introducing high performance P^+ back surface field behavior utilizes an aluminum paste which is caused to react with the silicon surface by a short high temperature firing operation. Other methods such as high temperature alloying of evaporated high purity aluminum or diffusion of boron into the silicon back surface have not resulted in satisfactory and reproducible BSF effect. Possibilities for employing ion implantation and/or pulsed electron beam processing to produce good back field effects were given preliminary examination under this program.

The back contact process used in fabricating test cells for this program could employ a thin evaporated aluminum film to be alloyed with the silicon at 650°C for 15 minutes prior to deposition of a standard back contact which was usually 400Å of aluminum followed by 1 μm of silver. The alloyed aluminum film insured good ohmic behavior under a wide range of operational environments but, by the process described, did not provide back field performance enhancement. It was anticipated that a set of ion implant and anneal parameters could be identified which would result in a satisfactory profile for field effect. Expectations were that the necessary implant would involve moderate fluence and reasonably high energy.

A number of tests were conducted using B^{11+}, BF_2^{49+} or Al^{27+} implants at several fluences up to a maximum of 10^{15} ions/cm^2. Pulsed electron beam annealing and furnace annealing at temperatures up to 850°C were investigated. No evidence of satisfactory BSF effect was observed. Tests were conducted with and without an alloyed aluminum layer under the back contact. Absence of BSF effect continued.

First evidence of a back field effect produced by ion implantation or a pulsed electron beam process was observed in a group of test cells to demonstrate total cell fabrication processing without any furnace operations. It was planned that these cells would have ion implanted, pulsed annealed junctions but no back layer implant. In order to produce good back surface ohmic contact without any conventional heat treatment, the first operation in the cell processing sequence was to evaporate 200Å of aluminum onto the wafer back surface. This surface was then subjected to an electron beam pulse to alloy the aluminum to form the underlayer for the contact to be added later after junction implant, implant damage pulse anneal, etc. It was observed that the group of 10 ohm-cm cells fabricated by this method exhibited an average of approximately 25 to 30 millivolts higher open circuit voltages than similar implanted, pulse annealed junction cells in which the P^+ back contact underlayer was produced by furnace alloying the 200A of aluminum at 650°C. The effect was found to be reproducible. Program limitations prevented further investigation and optimization of this pulsed electron beam alloying operation for back field introduction purposes. It is apparent that the rapidly induced, quickly quenched transient by an electron beam pulse is more than a simple replacement for a furnace alloying operation.

Following observation of back field effect caused by pulsed electron beam alloying of evaporated aluminum, it was found high fluence implants of boron or aluminum ions could also be used to produce BSF effects. While fluences of 10^{15} ions/cm^2 and less had previously not given positive results, fluences of 5×10^{15} ions/cm^2 at 10 to 25 keV were found to consistently result in at least substantial voltage enhancement following pulsed electron beam or 850°C furnace anneal. Schedule and funding limitations prevented additional investigation under this program.

4.2.3 Furnace Annealing of Ion Implantation Damage

The approach to cell development utilized under the program required initial cell structural investigations to be conducted using *furnace annealing of ion implantation damage.* This was necessitated by delays in developing electron beam pulse conditions which could be used for processing of high performance cells. It was planned that the cell structure could be developed using thermal processing, then reproduced and, if possible, improved by substituting pulsed electron beam annealing in place of furnace annealing.

Ions produce highly disordered region tracks as they penetrate into the material being implanted. The character of the damage produced and associated annealing requirements depend upon a number of parameters including ion specie, ion energy, ion fluence, substrate orientation and substrate temperature during implant. For implants conducted at room temperature there are three basic damage situations:

(1) Spatially separated disordered regions caused by low fluence implants.

(2) Amorphous layers due to overlapping disordered regions caused by high fluence implants.

(3) Overlapping disordered regions including some isolated undamaged material caused by intermediate fluence implants.

The isolated disorder regions caused by low fluence implants in silicon are generally rather easily annealed to restore single crystal structure. Amorphous layers caused by high fluence implants can be restored during annealing to single crystal silicon by epitaxial regrowth from the undamaged substrate below the implanted layer to the implant surface. The damage caused by intermediate fluence implants is such that restoration of single crystal material by thermal annealing is more difficult. When the implanted layer contains isolated undamaged regions, perhaps extremely small, competition during thermal anneal occurs between regrowth initiating at isolated crystal sites remaining within the implanted layer and

regrowth occuring epitaxially from undamaged crystal below the implanted layer. Unless thermal annealing is very carefully conducted, the resulting structure in this case is an annealed layer consisting of a matrix of polycrystallites.

The implants used for silicon solar cell structures are generally such as to be close to the threshold for amorphous layer creation. Consequently, when thermally annealed, they should be treated as intermediate fluence situations. Best available procedures for thermal annealing of almost amorphous layers involve a double step process.[20] A low temperature (450-550°C) step is first used to define the lattice structure regrowth with minimal competitive creation of polycrystallites. Then a higher temperature step (600-950°C) is used to complete the structure including activating the implanted dopant. Thermal annealing used for solar cell fabrication purposes under this program employed the two-step procedure. A typical anneal condition used for a junction and/or back surface implant was:

550°C	-	2 hours
850°C	-	15 minutes

in nitrogen. As was discussed in Section II, crystalline quality of implanted layers annealed by even double step thermal processing was inferior to that produced by pulsed electron beam annealing.

4.2.4 Contacts

A number of contact configurations and metallurgy systems were considered for use on developmental cells of this program. Because, as was discussed in Section 4.2.1, experimental cells actually had moderately deep (0.25-0.30 μm) junctions, few contacting problems were experienced.

Initial cell structures utilized front aluminum contacts evaporated through a mask. These aluminum front contacts were either deposited onto cell substrates at approximately 230°C or were deposited at room temperature and subsequently subjected to a short sintering cycle at approximately 400°C in forming gas.

Feasibility of performing the sintering operation using an electron beam pulse was demonstrated.

Because it was anticipated that the ability to apply contacts to junctions of less than 0.2 μm would be required, front contacts of aluminum were not expected to remain acceptable. The use of aluminum-2% silicon sputtered through a mask was investigated. Figure 20 shows I-V characteristics initially and after a series of 5 minute sintering cycles from a test cell structure with an implanted junction of depth approximately 0.2 μm onto which an aluminum-2% silicon contact grid had been sputtered. The data suggest that this contact material might be satisfactory even for shallow junctions. However, because of difficulties in sputtering the total thickness of a very fine grid structure for a high performance implanted cell, the Al-2% Si contact was not considered further.

Front contacts of cells produced during later phases of developmental work were applied using photolithographic processing of evaporated films followed by electroplating to build up grid line thickness. Contact systems employed were:

- Chromium-Gold-Silver
- Titanium-Silver
- Titanium-Palladium-Silver.

During the program, cell back contacts were aluminum, aluminum-silver or titanium-silver and sometimes included an aluminum film underlayer a few hundred angstoms thick deposited by evaporation, then alloyed to the silicon wafer. The alloying was usually performed in a furnace at 650°C for approximately 15 minutes. At times an electron beam pulse was employed and gave better results. However, only one experimental pulse generator was available for program studies. It was believed that its use for pulse alloying work could lead to contamination effects when utilized for implantation damage annealing. Because program emphasis was upon pulsed annealing of implantation damage, the electron beam pulser was employed only occasionally for contact studies and was thoroughly cleaned after each such use.

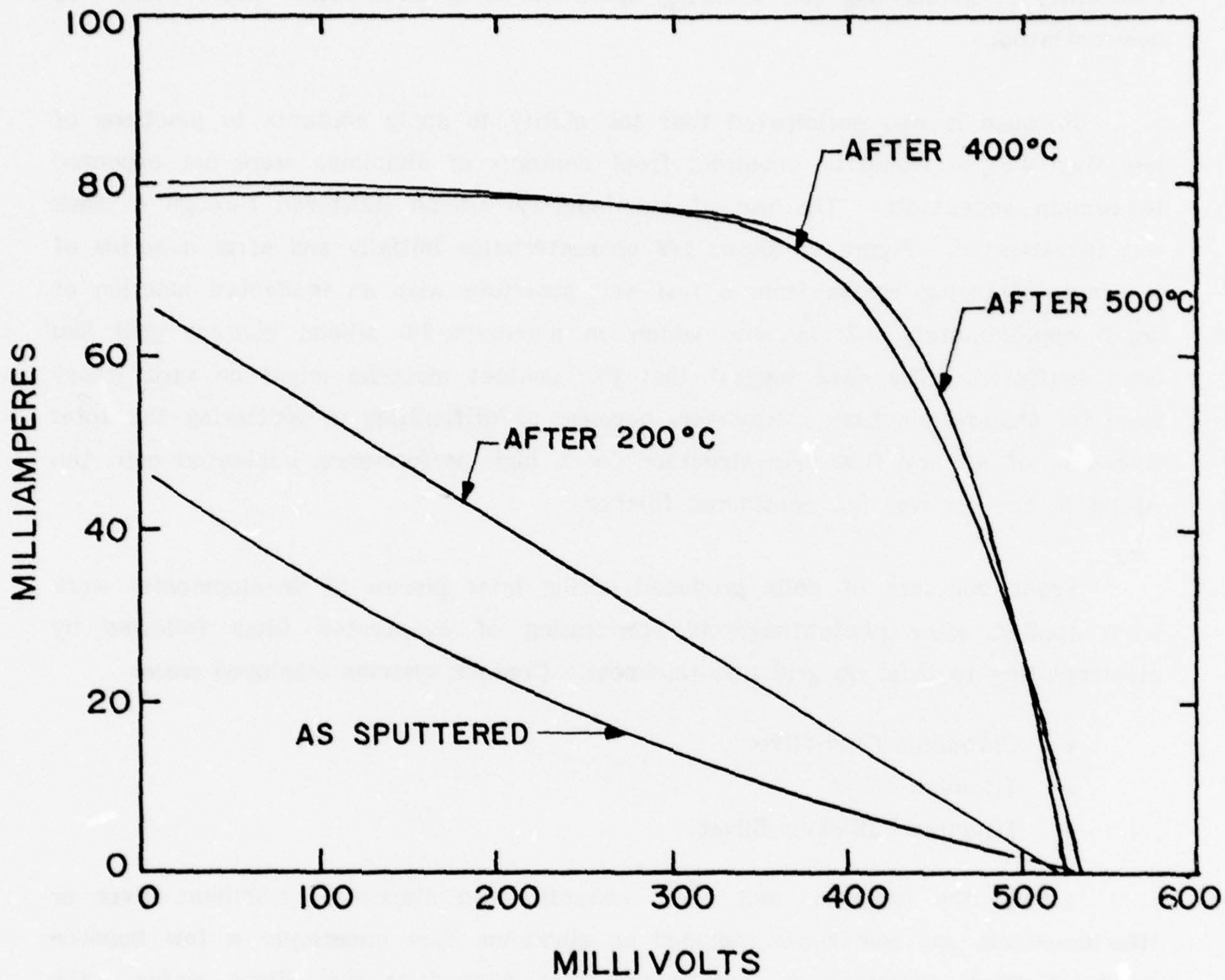


Figure 20. The Effect of Sequential 5 Minute Sintering Steps on Shallow Junction Test Cell with Al-2% Si Front Contact

The front contact pattern photomask prepared for 2x2cm cells is shown in Figure 21. As shown, the pattern involved 20 grid lines per centimeter and could be used for implanted junction layers with sheet resistance in excess of 200 ohms/□. A modified mask pattern was also prepared in which half the grid lines were removed. This 10 lines/cm version was adequate for most implanted junctions which had typical sheet resistance of approximately 100 ohms/□ .

4.2.5 Antireflection Coatings

Several candidate materials were considered for use as the solar cell single layer AR coating. The method used for coating deposition was vacuum evaporation using a DC electron beam. The evaporator employed was equipped to provide controlled residual pressure of oxygen. Some materials were subjected to post deposition heat treatment in oxygen. Factors considered in selection of an AR coating included:

- Refractive index of deposited material
- Optical absorption characteristics of deposited material
- Deposited coating physical stability
- Ease of deposition by electron beam evaporation.

Table 5 summarizes characteristics of the materials evaluated. Tested coatings were deposited onto fused silica slides. Refractive index measurements were made using a Gaertner ellipsometer.

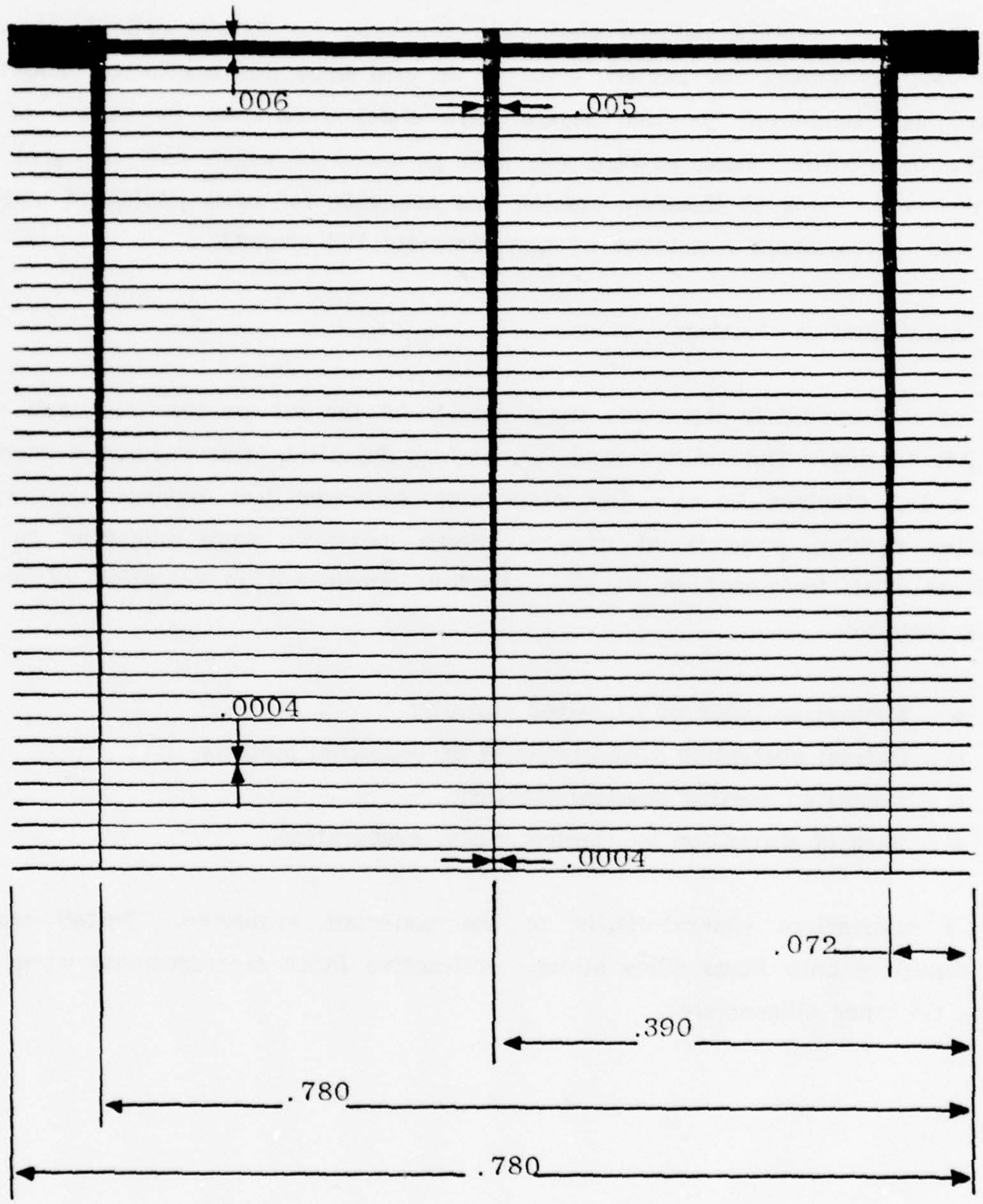


Figure 21. Photomask for 2 x 2 cm Cell

TABLE 5

Characteristics of Candidate AR Coating Materials

Material	Post Deposition Treatment	Measured Refractive Index at 633 nm	Visual Absorption	Ease of Evaporation
Ta_2O_5	None	1.96	Low	Good
Ta_2O_5	500^oC in O_2	2.01	Low	
Nb_2O_5	500^oC in O_2	2.07	Moderate	Difficult
Ti_2O_3	None	2.23	High	Fair
Ti_2O_3	500^oC in O_2	2.39	Moderate	
CeO_2	None	1.88	Moderate	Good
CeO_2	500^oC in O_2	1.83	Moderate	
ZrO_2-A	None	1.90	Low	Good
ZrO_2-A	500^oC in O_2	1.97	Low	
ZrO_2-B	None	1.63	Very Low	Excellent
ZrO_2-B	500^oC in O_2	1.69	Very Low	
TiO_2	None	2.16	Very Low	Excellent

Three materials were selected for further evaluation. First order red violet coatings of ZrO_2, Ta_2O_5 and TiO_2 were electron beam evaporated in 10^{-4} Torr residual oxygen onto uncoated production type diffused junction N/P cells at $250^{o}C$. Measured AM0 short circuit current data taken from the cells before and after coating are summarized in Table 6. Measurements were repeated on the ZrO_2 and TiO_2 cell groups after application of 7070 glass cover slides. Average total increase in short circuit current observed with the TiO_2 coating was 45% from the bare cells to AR coated cells with covers. Increases due to the other coating materials were lower. The TiO_2 was selected for use on developmental implanted junction cells. A test was conducted in which TiO_2 AR coatings were applied to sample 1 and 10 ohm-cm implanted junction cells. The results are summarized in Table 7. Relative effect of the TiO_2 coating on the implanted junction cells was very similar to that produced on the diffused junction cells as listed in Table 6.

4.3 Solar Cell Performance

Optimization of the implanted solar cell structure was not completed under this program, nor was optimization of the use of pulsed electron beams for solar cell processing purposes. Among the more serious remaining deficiencies of solar cell structure and processing are the following:

(i) Implanted junctions are too deep (0.25-0.30 μm) after pulse anneal or furnace anneal required for profile redistribution.

(ii) Implanted back surface layers produce only moderate performance enhancement characteristics; requirements for optimization have not yet been identified.

(iii) Front contact configuration and processing should be improved to reduce series resistance and shadowed area losses.

(iv) Silicon type/resistivity have not yet been selected on basis of experimental optimizations.

TABLE 6

Summary of AR Coating Evaluation on Diffused Junction Cells

Coating Material	Number of Cells Coated	Average I_{sc} Initially	Average I_{sc} After Coating	Percent Increase	Average I_{sc} With Cover	Total Percent Increase
ZrO_2-A	8	94 mA	119 mA	27	121 mA	29
Ta_2O_5	8	102	135	32	Not Measured	
TiO_2	5	94	130	38	136	45

TABLE 7

Effect of TiO_2 AR Coating on Implanted Junction Cells

Silicon Resistivity (ohm-cm)	Cell	Performance Uncoated		Performance with TiO_2	
		V_{oc} (mV)	I_{sc} (mA)	V_{oc} (mV)	I_{sc} (mA)
10	A	540	102	550	140
	B	540	103	550	240
	C	540	104	550	145
1	A	565	99	573	136
	B	555	99	568	138
	C	560	96	570	134

(v) Furnace annealing necessary for implant damage removal plus dopant redistribution requires excessive temperature ($850^{o}C$).

(vi) Pulsed electron beam annealing for junction implant anneal has not yet been optimized with respect to dopant redistribution.

(vii) Requirements for pulsed electron beam processing of back surface layers have not yet been identified.

In spite of these shortcomings, the status of ion implanted silicon solar cells has been substantially advanced and the concept of pulsed energy processing has been shown to be viable for solar cell processing purposes. Ion implanted silicon solar cells with performance characteristics comparable to those of state-of-the-art diffused junction cells can now be produced.

Figure 22 shows the AM0 I-V characteristic of a 2 x 2cm planar surface N^{+}/PP^{+} cell with implanted junction and back surface layers. Both implants were simultaneously annealed in a furnace. Efficiency of the 10 ohm-cm <100> CG silicon cell shown was 13.7% AM0. The processing used for cells with furnace annealed implants was as follows:

Implant front:	P^{31+}, 10 keV, 2.5×10^{15} cm^{-2}
Implant back:	B^{11+}, 25 keV, 5×10^{15} cm^{-2}
Anneal in N_2:	2 hours at $550^{o}C$ 15 minutes at $850^{o}C$
Apply front contact:	400Å Cr + 400Å Au + 3 μm Ag
Apply back contact:	400Å Al + 1 μm Ag
Apply AR coating:	700Å TiO_2
Sinter in N_2	10 minutes at $400^{o}C$

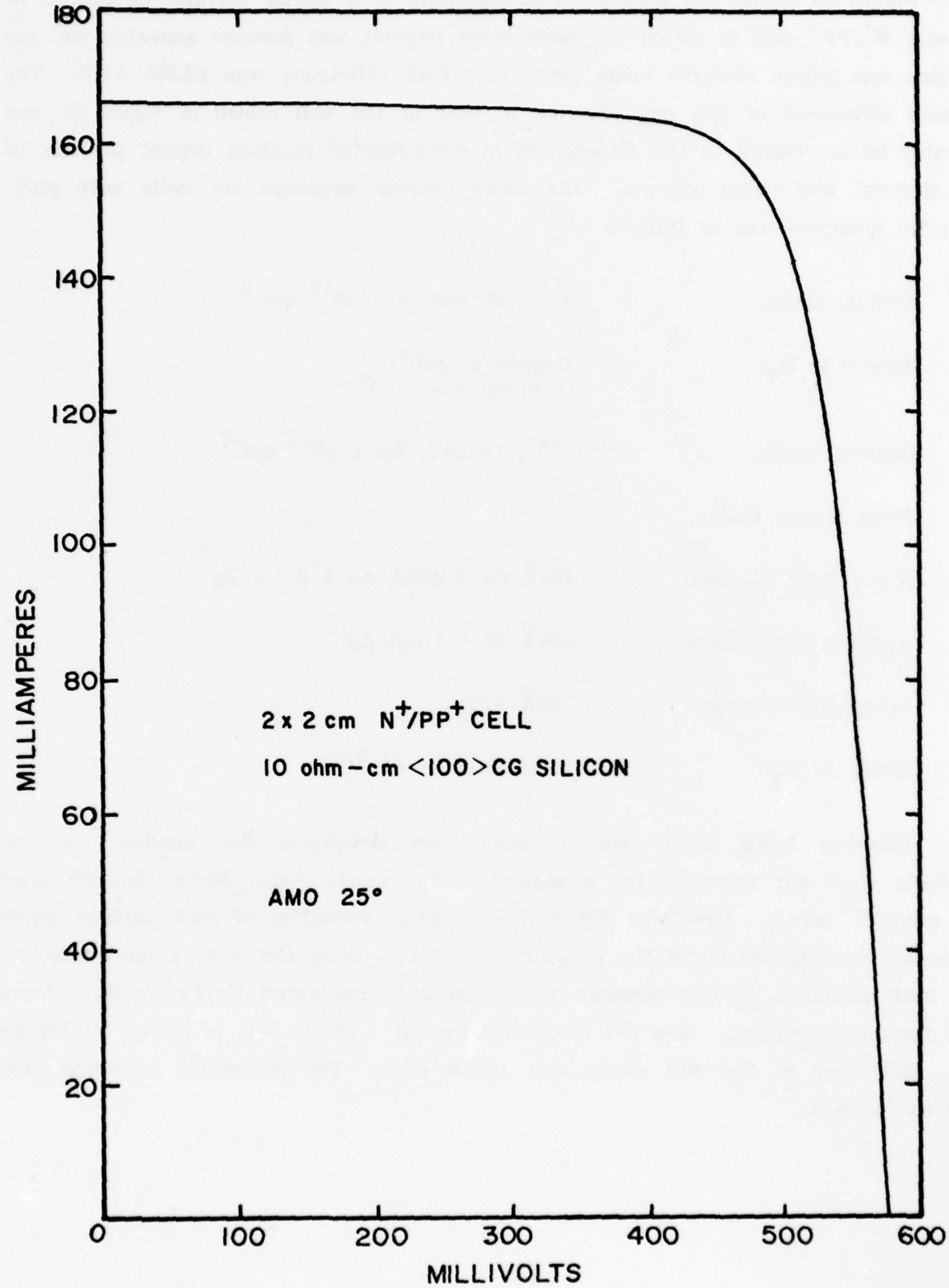


Figure 22 . AMO I-V Characteristic of Implanted/Furnace Annealed Cell

Figure 23 shows the AM0 I-V characteristic of a planar surface implanted 10 ohm-cm N^+/PP^+ cell in which the back layer implant was furnace annealed and the junction was pulsed electron beam annealed. Cell efficiency was 12.9% AM0. The reduced *efficiency* of this cell relative to that of the cell shown in Figure 22 can probably be attributed to the differences in redistributed junction dopant profiles of the thermal and pulse anneals. The basic process sequence for cells with pulse annealed junctions was as follows:

Implant back:	B^{11+}, 25 keV, 5×10^{15} cm^{-2}
Anneal in N_2:	2 hours at 550°C 15 minutes at 850°C
Implant front:	P^{31+}, 10 keV, 2.5×10^{15} cm^{-2}
Pulse anneal front:	
Apply front contact:	400Å Cr + 400Å Au + 3 μm Ag
Apply back contact:	400Å Al + 1 μm Ag
Apply AR coating:	700Å TiO_2
Sinter in N_2:	10 minutes at 400°C

Electron beam pulse anneal parameters developed for shallow junction implants were not adequate for annealing of the much deeper boron implants used for back P^+ layers. Condition for optimized pulse annealing of back surface layers were not investigated under the program. However, using the same pulse conditions for both implants, it was possible to demonstrate implanted N^+/PP^+ cells without any furnace annealing. The I-V characteristic of such a cell is shown in Figure 24. Efficiency of the cell shown was 11.9% AM0. The processing sequence used was as follows:

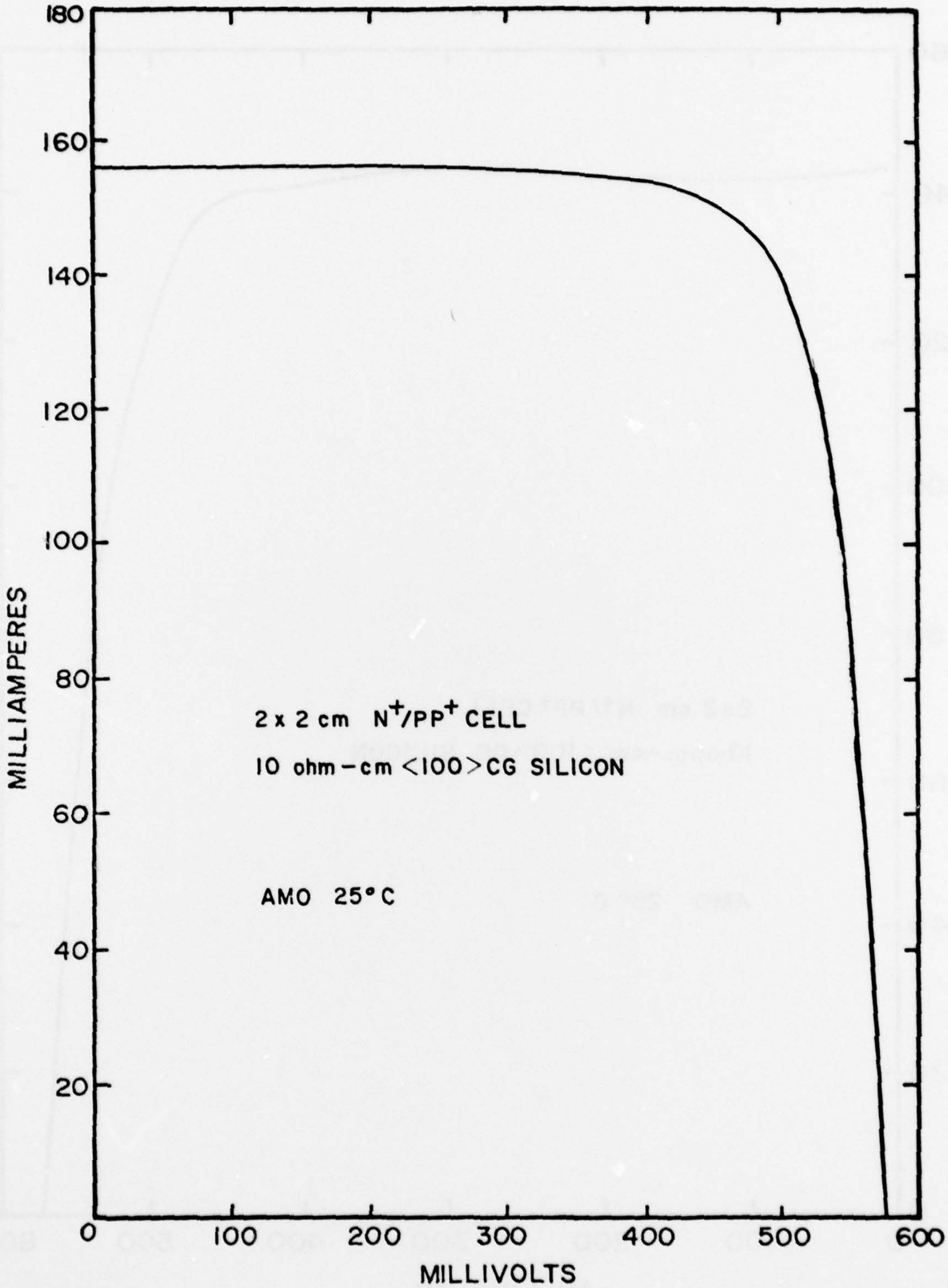


Figure 23. AMO I-V Characteristic of Implanted Cell with Pulsed Electron Beam Annealed Junction

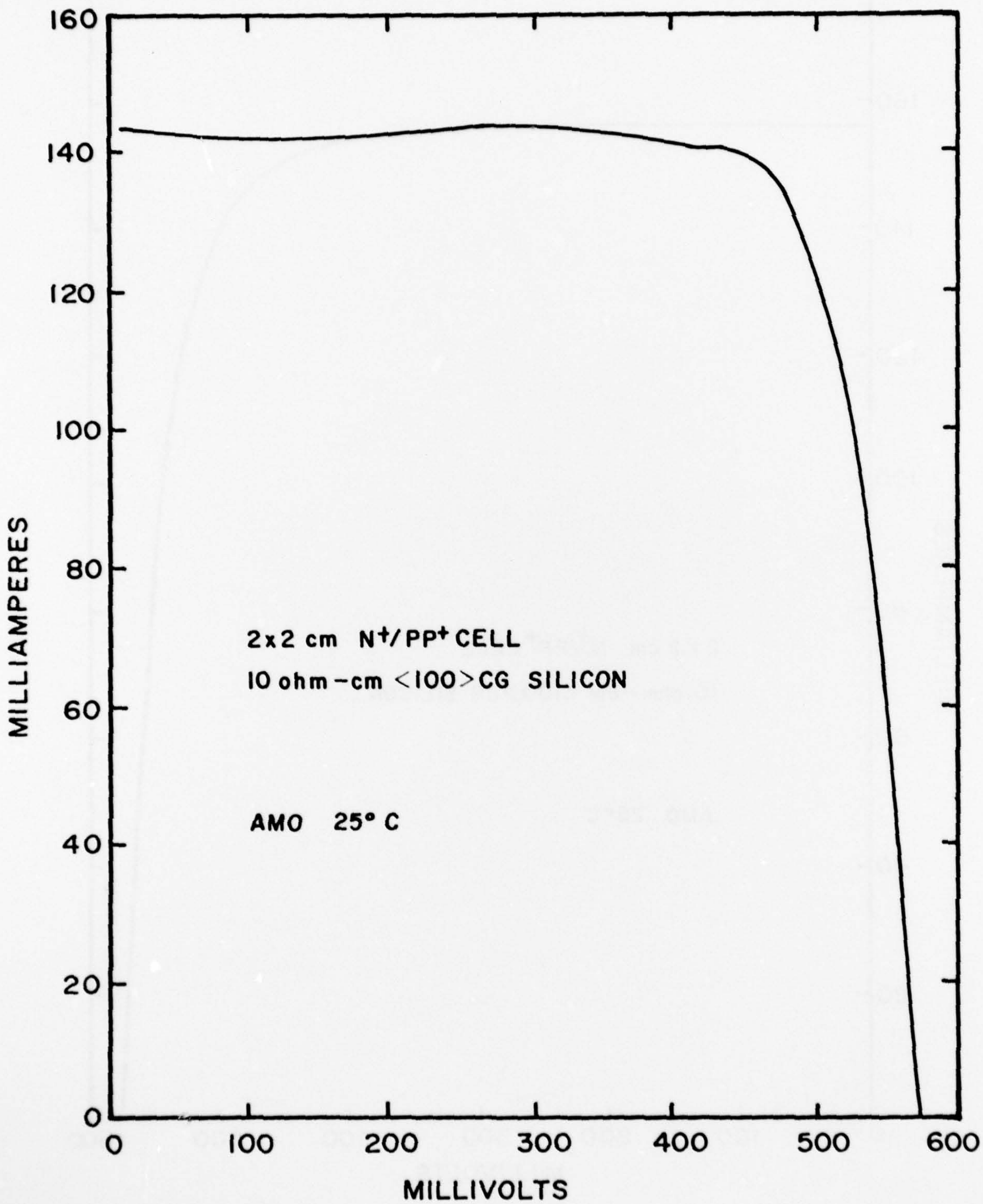


Figure 24. AMO I-V Characteristic of Implanted Cell with Pulsed Electron Beam Annealed Junction and Back Layer

Implant back:	B^{11+}, 25 keV, 5×10^{15} cm^{-2}
Pulse anneal back:	
Implant front:	P^{31+}, 10 keV, 2.5×10^{15} cm^{-2}
Pulse anneal front:	
Apply front contact:	400Å Cr + 400Å Au + 3 μm Ag
Apply back contact:	400Å Al + 1 μm Ag
Apply AR coating:	700A TiO_2
Sinter in N_2:	10 minutes at 400°C

The cells represented in Figures 22, 23 and 24 had planar surface junction. Utilization of ion implantation for cells with texturized front surfaces was also of interest. A single group of texturized surface 10 ohm-cm cells was prepared. Surface texturizing was performed using a commercial hydrazine etch. No implant was used on the cell back surfaces and they consequently showed no open circuit voltage enhancement. The junction implants were performed in four steps so that the wafers were tilted relative to the ion beam to expose each of the pyramidal faces separately. Figure 25 shows the AM0 I-V characteristic of one of the texturized surface implanted cells without AR coating. The result suggests that high efficiency ion implanted texturized surface cells would be easily developed.

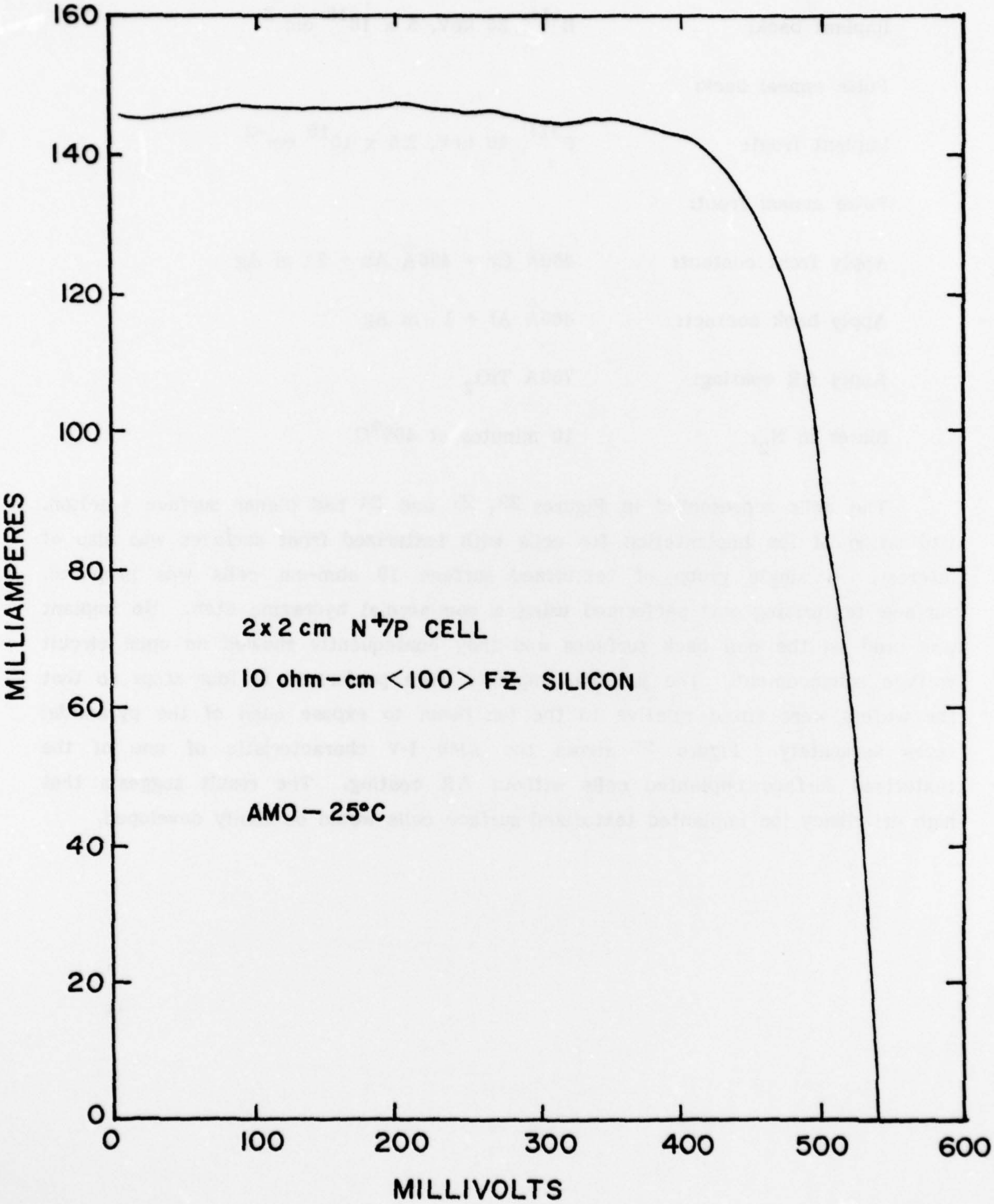


Figure 25. AMO I-V Characteristic of Implanted Texturized Surface Cell

SECTION V

ELECTRON IRRADIATION STUDY

As was discussed in Section 3.3.2, during this program AFAPL supplied two sets of test samples to Rome Air Development Center, Hanscom AFB, MA, for investigation by transient capacitance spectroscopy to detect processing-induced defects.[(4)] P.J. Drevinsky, J.T. Schott and H.M. DeAngelis of RADC were able to provide evidence of junction region contamination involving the pulsed electron beam and were a year later able to confirm that the contamination problem had been eliminated. For the second series of evaluations, otherwise identical cells were specially prepared by Spire with diffused junctions, ion implanted furnace annealed junctions, and ion implanted pulse annealed junctions. Transient capacitance studies were conducted upon samples of these cells before and after irradiation by 1 MeV electrons. Differences were observed in the relative degree of radiation induced performance degradation incurred by cells with different methods of junction formation.

Irradiations were performed on 10 ohm-cm N^+/PP^+ cells fabricated from the same <100>CG silicon material. Air Mass Zero I-V curves were taken initially and after 1 MeV electron irradiation on a Dynamitron at RADC to fluences of 2×10^{15} and $1 \times 10^{16} cm^{-2}$. Cell data are summarized in Table 8. Irradiation induced the least degradation in the pulse annealed implanted junction cells and the most degradation in the diffused junction cells. Normalized maximum power data are plotted in Figure 26 .

Drevinsky, Schott and DeAngelis have speculated that solar cell radiation-induced degradation may involve processing-induced defects. If so, it is possible that low temperature cell fabrication methods based upon ion implantation and pulsed electron beam processing might offer prospects for cells with improved radiation tolerance.

TABLE 8

AMO Characteristics of 10 ohm-cm 2 x 2cm Cells Before and After Electron Irradiation

Fluence (e^-/cm^2)	Cell Parameter	Cell Type: Implanted Junction Pulse Annealed	Implanted Junction Furnace Annealed	Diffused Junction
0	I_{sc} (mA)	143	146	134
	V_{oc} (mV)	565	575	582
	P_{max} (mW)	62.0	65.6	60.0
2×10^{15}	I_{sc} (mA)	111	114	97.5
	V_{oc} (mV)	490	495	490
	P_{max} (mW)	40.4	40.4	33.8
1×10^{16}	I_{sc} (mA)	106	107	92.0
	V_{oc} (mV)	475	458	460
	P_{max} (mW)	36.9	37.0	30.4

AMO 25°C

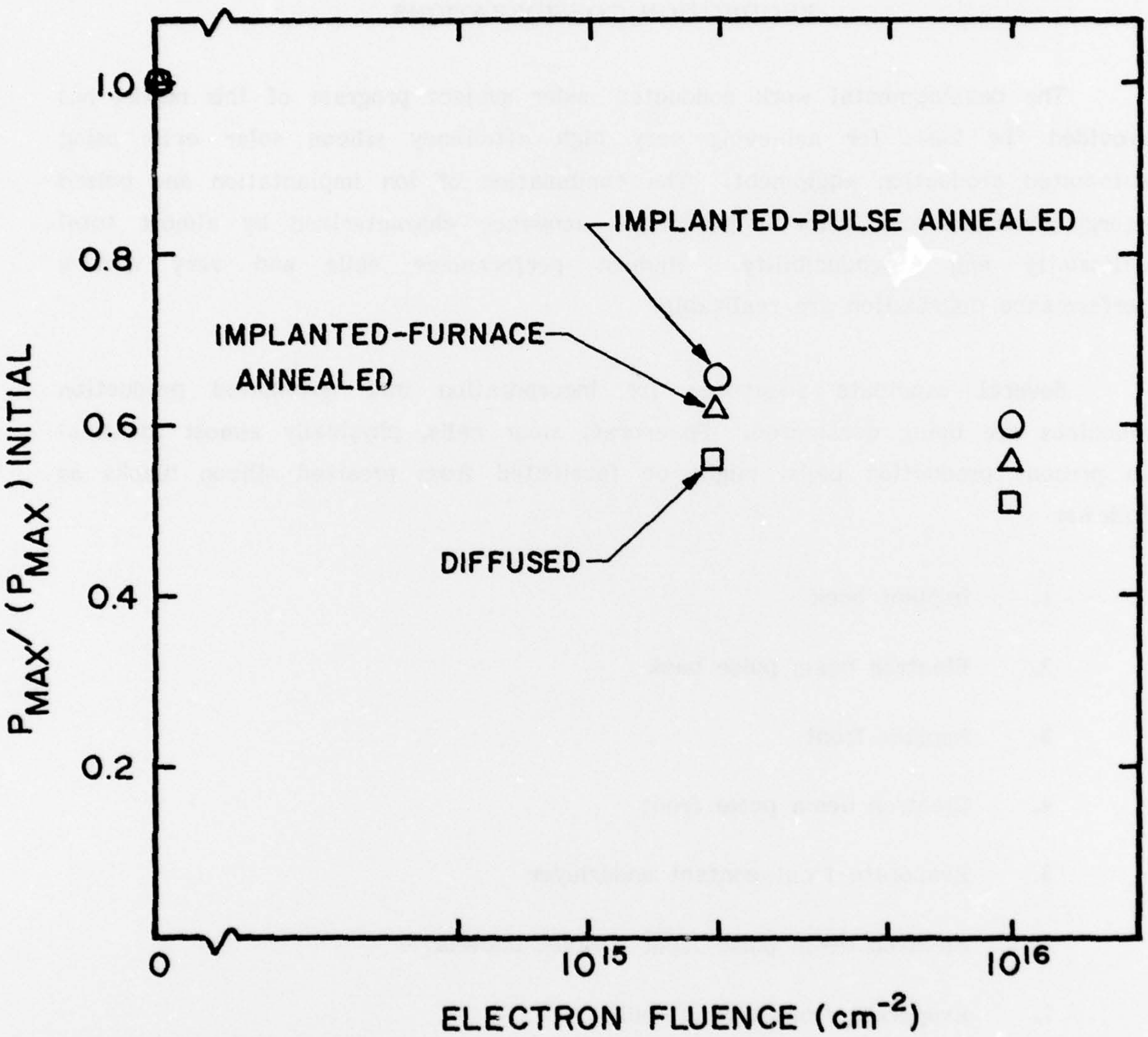


Figure 26. Normalized Cell Maximum Power Versus 1-MeV Electron Fluence

SECTION VI

PRODUCTION CONSIDERATIONS

The developmental work conducted under subject program of this report has provided the basis for achieving very high efficiency silicon solar cells using automated production equipment. The combination of ion implantation and pulsed energy processes can offer a production sequence characterized by almost total uniformity and reproducibility. Highest performance cells and very narrow performance distribution are realizable.

Several candidate sequences for incorporation into automated production machines are being considered. Spacecraft solar cells, physically almost identical to present production cells, might be fabricated from presized silicon blanks as follows:

1. Implant back
2. Electron beam pulse back
3. Implant front
4. Electron beam pulse front
5. Evaporate front contact underlayer
6. Electron beam pulse front contact underlayer
7. Evaporate front contact bulk
8. Evaporate back contact underlayer
9. Electron beam pulse back contact underlayer
10. Evaporate back contact bulk
11. Evaporate AR coating

A number of simplifications to the above sequence are possible. All of the steps required are "line of sight" procedures which can be conducted under vacuum at ambient or slightly elevated temperature. No wet chemistry or gas phase operations are needed. Very high production throughput rates with minimal processing waste generation are possible.

The approach to solar cell processing which was initiated under this contract is now being utilized by Spire for development of terrestrial solar cell automated production technology under the Large Scale Solar Array Project being conducted by Jet Propulsion Laboratory for the U.S. Department of Energy.[21] In support of automated production development for the LSA Project, Spire has installed, and is now operating, a first high throughput solar cell process ion implanter. This implanter is capable of performing junction or back layer implants into 300 4-inch wafer per hour. In terms of 2 x 2cm spacecraft solar cells, throughput capacity of the implanter would be of the order of 3000 cells per hour. A high volume production implanter able to process 180 m^2 of solar cell surface per hour has been designed. Electron beam pulsers for solar cell processing to be compatible with such a machine are being developed.

SECTION VII

CONCLUSION

This program has resulted in the development of combined ion implantation/pulsed electron beam processing techniques. The work was very successful in preparing technology which should have important future applications to solar cell production and to production of other semiconductor devices.

Integration of ion implantation and pulsed energy into a complete solar cell fabrication approach has been shown to have real potential for achieving solar cell performance beyond present limits. Ion implantation/pulsed processing methods have been demonstrated to produce junction layers free of polycrystallites and even dislocations. It has been shown that all of the processes necessary to fabricate a high performance N^+/PP^+ silicon solar cell structure can be accomplished without subjecting the solar cell base region to elevated temperatures. Prospects for enhancement of minority carrier lifetimes to achieve improved response are excellent.

Advances were made in the state-of-the-art of ion implanted solar cells. Optimization of the cell structure was not completed, but planar surface cells with efficiencies up to 13.7% AM0 were fabricated. The use of implantation for texturized surface cells was demonstrated. Back surface field effects were achieved. Requirements for further technical development to accomplish higher efficiencies were identified.

The technology which was developed is extremely adaptable to automated production of solar cells. The use of ion implantation and pulsed electron beam processing can allow low cost, high speed production of high performance cells with very narrow performance distributions.

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